



General Description

AFE0504 are designed by bi-direction TVS diode, to protect high speed data interfaces. This product has been specifically designed to protect sensitive components which are connected to data and transmission lines from overvoltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients). The TVS diode prevents over-voltage on the power line, protecting any downstream components. The low capacitance configuration allows the user to protect high-speed data or transmission lines. This device is optimized for ESD protection of portable electronics. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

Features

- Transient protection for high-speed data lines to IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 8\text{kV}$ (contact) IEC 61000-4-4 (EFT) 40A (5/50ns)
- Small package saves board space
- Protects up to four I/O lines & power line
- Low capacitance (<3pF) for high-speed interfaces
- Low leakage current and clamping voltage
- Low operating voltage: 5.0V
- Solid-state silicon-avalanche technology

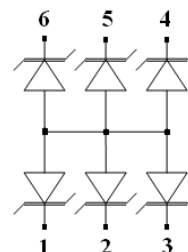
Application

- USB 2.0 Power and Data Line Protection
- Monitors and Flat Panel Displays
- Digital Visual Interface (DVI)
- 10/100/1000 Ethernet
- Notebook Computer
- SIM Ports
- ATM Interface
- IEEE 1394 Firewire Ports
- Cellular Handsets & Accessories
- Portable Instrumentation
- Digital Cameras
- MP3 Players
- Video Graphics Cards

Pin Description (SOT-363)



Schematic & PIN Configuration(SOT-363)



Ordering Information

| Part Ordering No. | Part Marking | Package | Unit | Quantity |
|-------------------|--------------|---------|-------------|----------|
| AFE0504S36RG | E4YW | SOT-363 | Tape & Reel | 3000 EA |

- ※ E4 parts code
- ※ Y year code (0 ~ 9)
- ※ W week code (A ~ Z = 1 ~ 26 / a ~ z = 27 ~ 52)
- ※ AFE0504S36RG : 7" Tape & Reel ; Pb- Free ; Halogen- Free



ABSOLUTE MAXIMUM RATINGS

(T_A=25°C Unless otherwise noted)

| Parameter | Symbol | Typical | Unit |
|---|------------------|---------------|------|
| Peak Pulse Power (t _p = 8/20 μs) | P _{pk} | 150 | W |
| Maximum Peak Pulse Current (t _p = 8/20 μs) | I _{PP} | 6 | A |
| ESD per IEC 61000 – 4 – 2 (Air) | V _{PP} | ±15 | KV |
| ESD per IEC 61000 – 4 – 2 (Contact) | V _{PP} | ±8 | KV |
| Operating Junction Temperature | T _J | -55 ~ 125 | °C |
| Storage Temperature Range | T _{STG} | -55 ~ 150 | °C |
| Lead Soldering Temperature | T _L | 260 (10sec) | °C |

ELECTRICAL CHARACTERISTICS

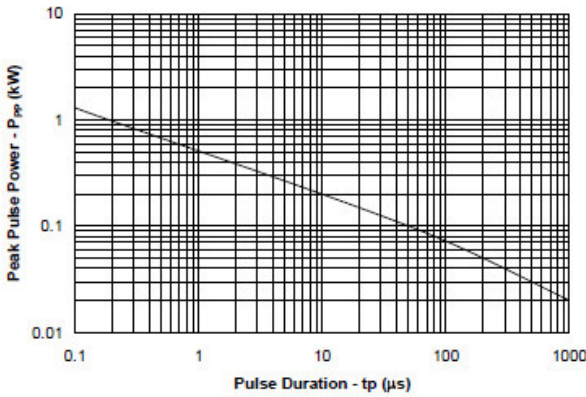
(T_A=25°C Unless otherwise noted)

| Parameter | Symbol | Conditions | Min. | Typ | Max. | Unit |
|-----------------------------|------------------|---|------|-----|------|------|
| Reverse Stand – Off Voltage | V _{RWM} | Pin 1 to 2 or 2 to 1 | | | 5 | V |
| Reverse Breakdown Voltage | V _{BR} | I _t = 1mA | 6 | | | V |
| Reverse Leakage Current | I _R | V _{RWM} = 5V , T=25°C | | 0.5 | 1 | μA |
| Clamping Voltage | V _C | I _{PP} = 1A , t _p = 8/20 μs Pin 1 to 2 or 2 to 1 | | | 13 | V |
| Clamping Voltage | V _C | I _{PP} = 6 , t _p = 8/20 μs Pin 1 to 2 or 2 to 1 | | | 15 | V |
| Junction Capacitance | C _j | V _R = 0V , f = 1MHz | | 2 | 3 | pF |

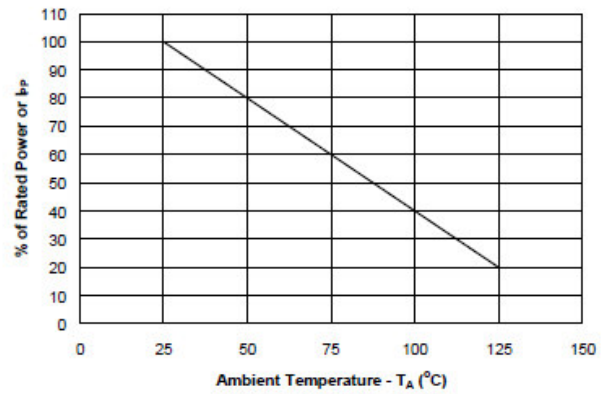


Typical Characteristics

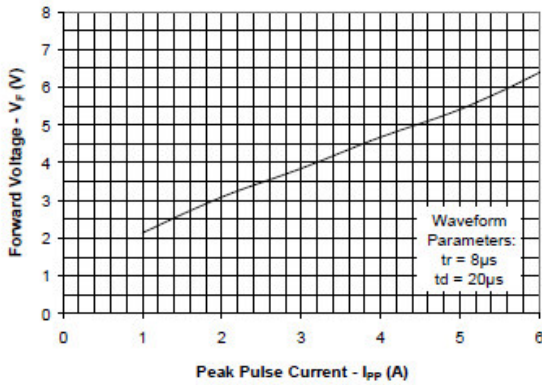
Non-Repetitive Peak Pulse Power vs. Pulse Time



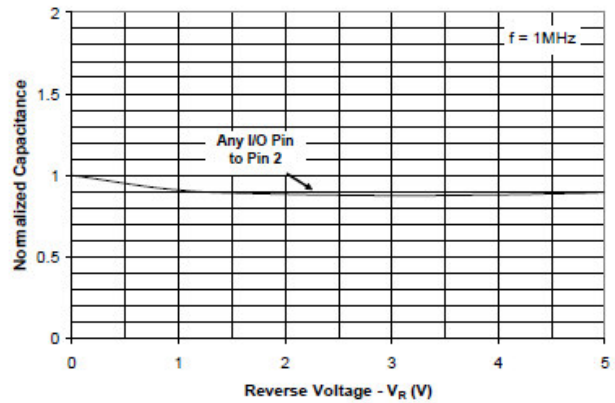
Power Derating Curve



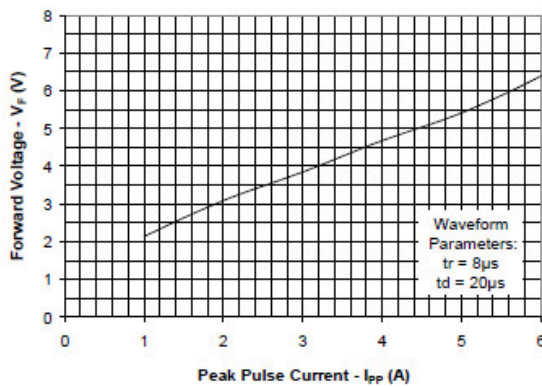
Forward Voltage vs. peak Pulse Current



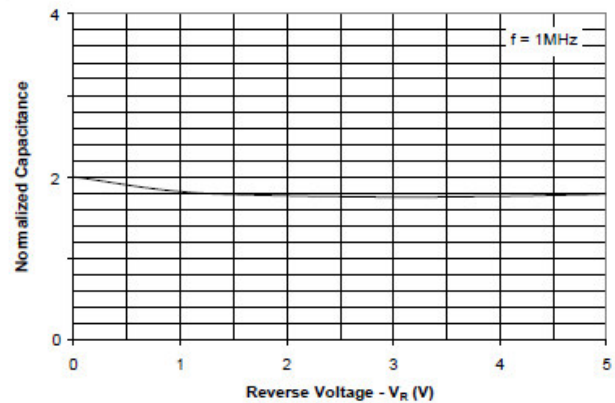
Capacitance vs. Reverse Voltage (Normalized to 0V)



Forward Voltage vs. peak Pulse Current



Capacitance vs. Reverse Voltage (Normalized to 0V)



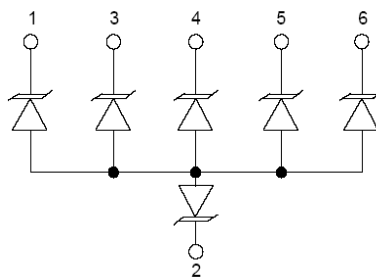


Application Information

Device Connection for Protection of Five Data Lines

AFE0504 is designed to protect up to five bidirectional data lines. The device is connected as follows:

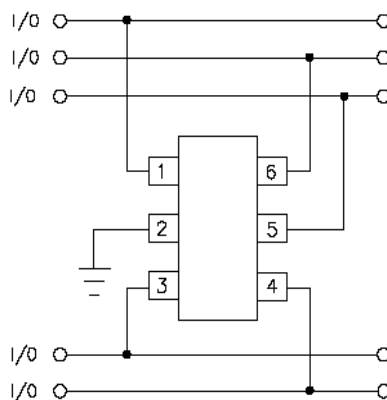
1. Bidirectional protection of five I/O lines is achieved by connecting pins 1, 3, 4, 5, and 6 to the data lines. Pin 2 is connected to ground. The ground connection should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.



Circuit Board Layout Recommendations for Suppression of ESD

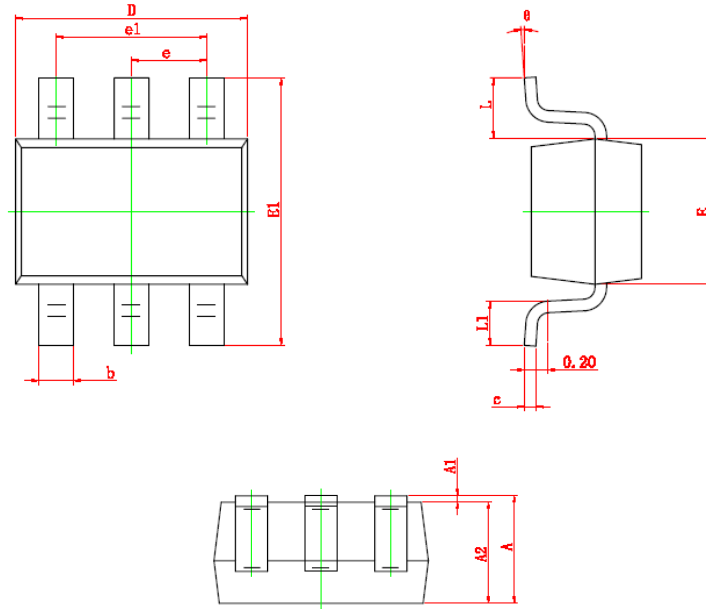
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

1. Place the TVS near the input terminals or connectors to restrict transient coupling.
2. Minimize the path length between the TVS and the protected line.
3. Minimize all conductive loops including power and ground loops.
4. The ESD transient return path to ground should be kept as short as possible.
5. Never run critical signals near board edges.
6. Use ground planes whenever possible.





Package Information (SOT-363)



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 0.900 | 1.100 | 0.035 | 0.043 |
| A1 | 0.000 | 0.100 | 0.000 | 0.004 |
| A2 | 0.900 | 1.000 | 0.035 | 0.039 |
| b | 0.150 | 0.350 | 0.006 | 0.014 |
| c | 0.080 | 0.150 | 0.003 | 0.006 |
| D | 2.000 | 2.200 | 0.079 | 0.087 |
| E | 1.150 | 1.350 | 0.045 | 0.053 |
| E1 | 2.150 | 2.450 | 0.085 | 0.096 |
| e | 0.650 TYP | | 0.026 TYP | |
| e1 | 1.200 | 1.400 | 0.047 | 0.055 |
| L | 0.525 REF | | 0.021 REF | |
| L1 | 0.260 | 0.460 | 0.010 | 0.018 |
| θ | 0° | 8° | 0° | 8° |

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