



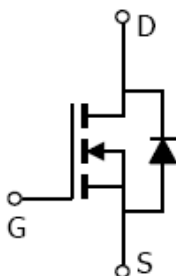
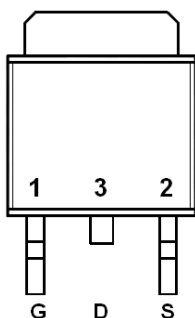
General Description

AFN2014, N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge. These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

Features

- 20V/ 10A, $R_{DS(ON)}=14m\Omega@V_{GS}=4.5V$
- 20V/ 8A, $R_{DS(ON)}=17m\Omega@V_{GS}=2.5V$
- 20V/ 5A, $R_{DS(ON)}=21m\Omega@V_{GS}=1.8V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- TO-252-2L package design

Pin Description (TO-252-2L)



Application

- Power Management in Desktop Computer
- DC/DC Converter
- LCD Display inverter

Pin Define

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFN2014T252RG	2014	TO-252-2L	Tape & Reel	2500 EA

- ※ A Lot code
- ※ B Date code
- ※ AFN2014T252RG : 13" Tape & Reel ; Pb- Free ; Halogen -Free



Absolute Maximum Ratings

($T_A=25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	20	V
Gate-Source Voltage	V_{GSS}	± 12	V
Continuous Drain Current($T_J=150^\circ\text{C}$)	I_D	$T_A=25^\circ\text{C}$	20
		$T_A=70^\circ\text{C}$	16
Pulsed Drain Current	I_{DM}	50	A
Continuous Source Current(Diode Conduction)	I_S	9.0	A
Power Dissipation	P_D	$T_A=25^\circ\text{C}$	40
		$T_A=70^\circ\text{C}$	15
Operating Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55/150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

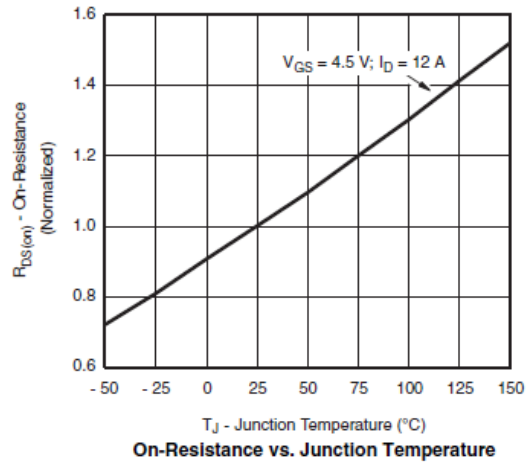
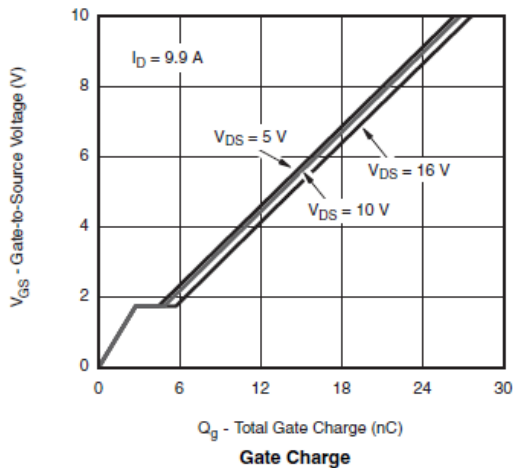
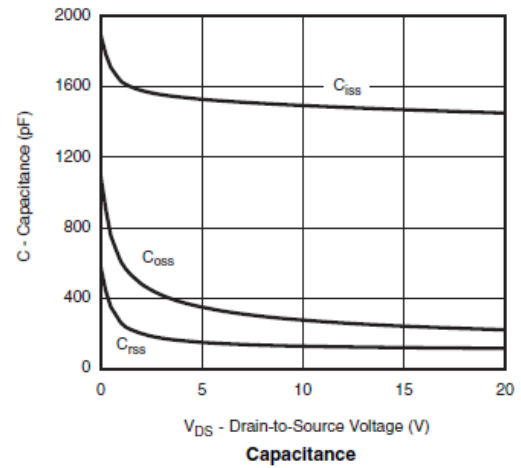
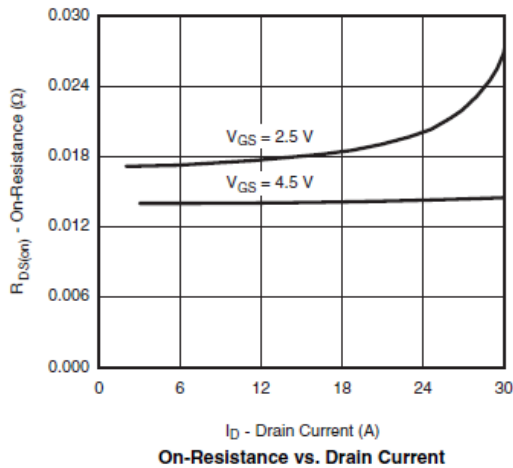
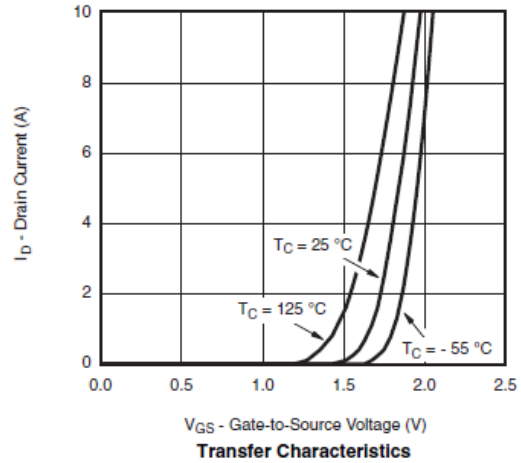
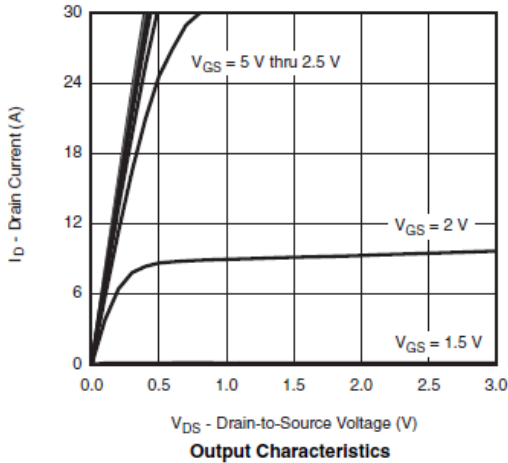
Electrical Characteristics

($T_A=25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu\text{A}$	20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.4		1.0	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 12V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$			1	uA
		$V_{DS}=20V, V_{GS}=0V$ $T_J=85^\circ\text{C}$			10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 5V, V_{GS}=4.5V$	30			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=10A$		11	14	m Ω
		$V_{GS}=2.5V, I_D=8A$		14	17	
		$V_{GS}=1.8V, I_D=5A$		17	21	
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=7.0A$		40		S
Diode Forward Voltage	V_{SD}	$I_S=5.0A, V_{GS}=0V$		0.8	1.3	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=10V, V_{GS}=4.5V$ $I_D=9.0A$		13	19	nC
Gate-Source Charge	Q_{gs}			2.8		
Gate-Drain Charge	Q_{gd}			2.0		
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V$ $f=1\text{MHz}$		1450		pF
Output Capacitance	C_{oss}			285		
Reverse Transfer Capacitance	C_{rss}			145		
Turn-On Time	$t_{d(on)}$	$V_{DD}=10V, R_L=1.3\Omega$ $I_D=8.0A, V_{GEN}=10V$ $R_G=1\Omega$		10	20	ns
	t_r			10	20	
Turn-Off Time	$t_{d(off)}$			25	40	
	t_f			10	20	

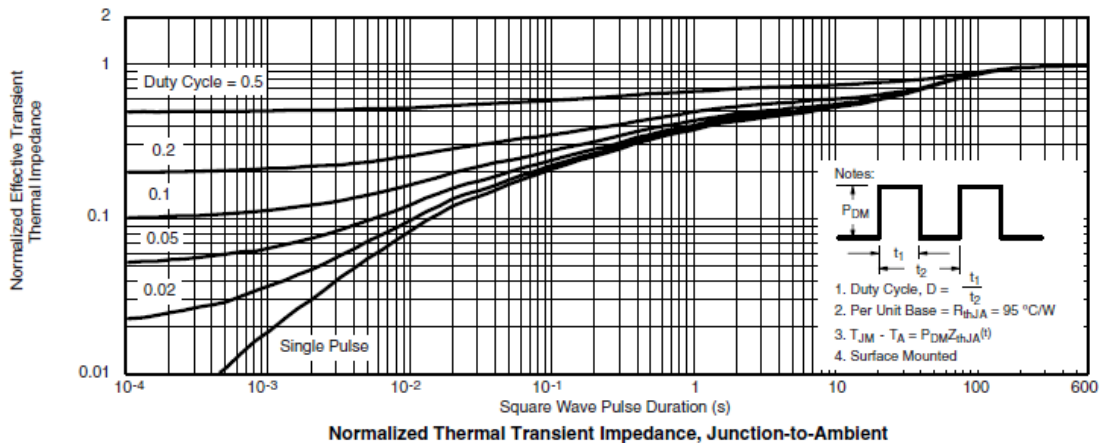
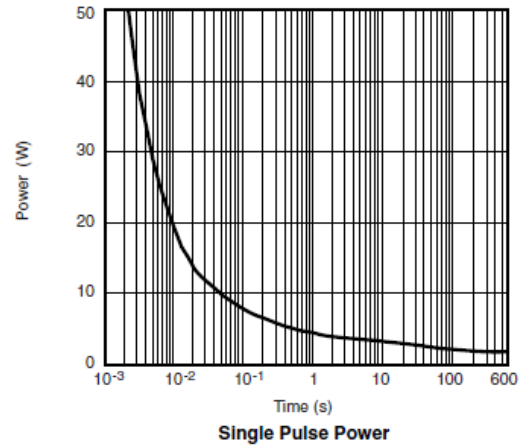
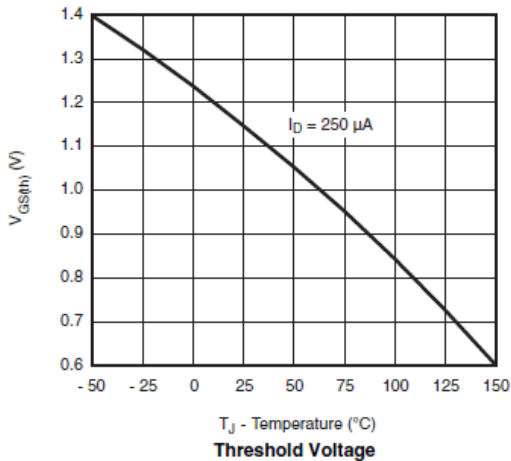
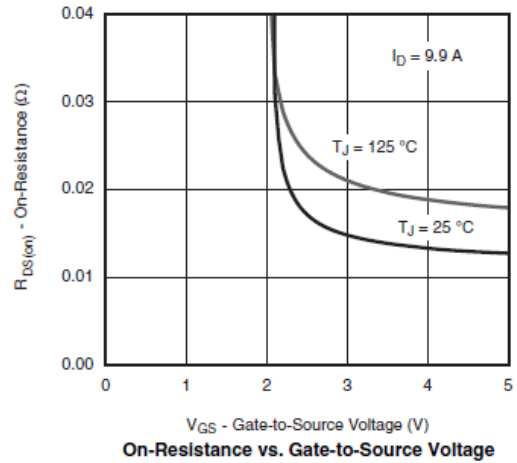
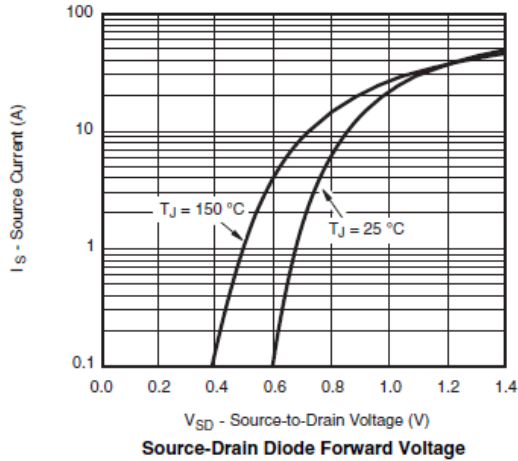


Typical Characteristics





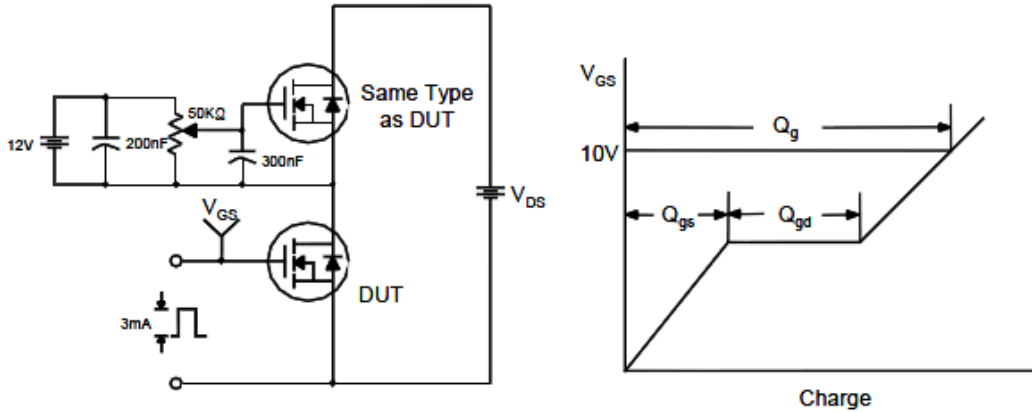
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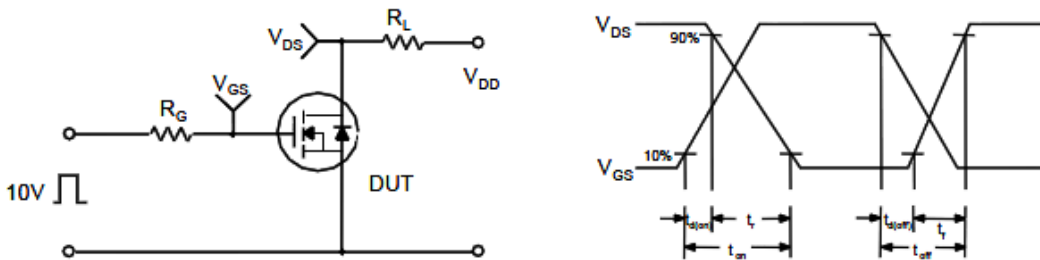


Typical Characteristics

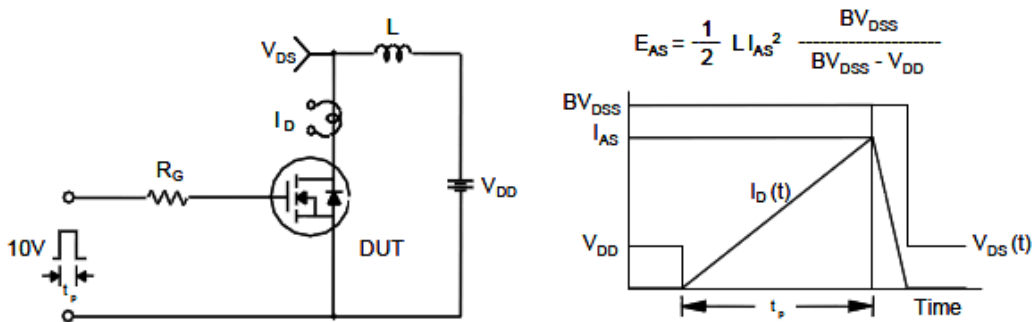
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

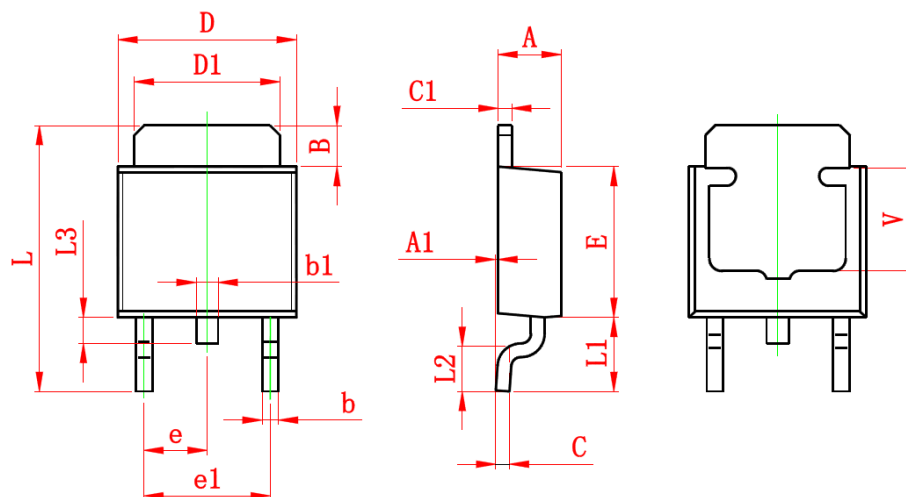


Unclamped Inductive Switching Test Circuit & Waveforms





Package Information (TO-252-2L)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP.		0.091 TYP.	
e1	4.500	4.700	0.177	0.185
L	9.500	9.900	0.374	0.390
L1	2.550	2.900	0.100	0.114
L2	1.400	1.780	0.055	0.070
L3	0.600	0.900	0.024	0.035
V	3.800 REF.		0.150 REF.	

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