



General Description

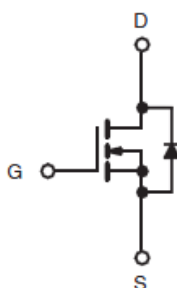
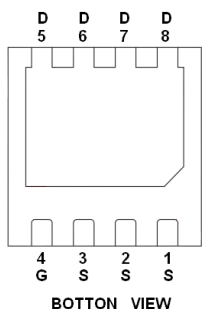
AFN3316W, N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

Features

- 60V/8A, $R_{DS(ON)}=140m\Omega@V_{GS}=10V$
- 60V/6A, $R_{DS(ON)}=148m\Omega@V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- DFN3X3-8L package design

Pin Description (DFN3X3-8L)



Application

- DC/DC Converter
- Load Switch
- Power Management in Notebook Computer

Pin Define

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFN3316WFN338RG	AFN3316W YYMMDD	DFN3X3-8L	Tape & Reel	5000 EA

- ※ YY year code
- ※ MM month code
- ※ DD date code
- ※ AFN3316WFN338RG : 13" Tape & Reel ; Pb- Free ; Halogen -Free



Absolute Maximum Ratings

($T_A=25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	V
Gate –Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current($T_J=150^\circ\text{C}$)	I_D	$T_A=25^\circ\text{C}$	8
		$T_A=70^\circ\text{C}$	6
Pulsed Drain Current	I_{DM}	10	A
Continuous Source Current(Diode Conduction)	I_S	1.6	A
Power Dissipation	P_D	$T_C=25^\circ\text{C}$	28
		$T_C=70^\circ\text{C}$	15
		$T_A=25^\circ\text{C}$	3.2
		$T_A=70^\circ\text{C}$	2.0
Operating Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55/150	$^\circ\text{C}$
Thermal Resistance Junction-to-Case (Drain)	$R_{\theta JC}$	5	$^\circ\text{C}/\text{W}$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	40	

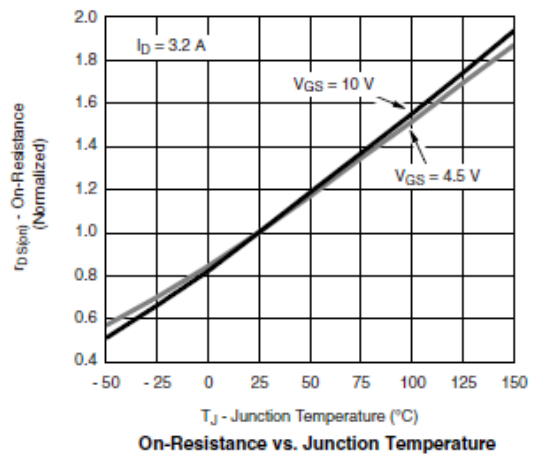
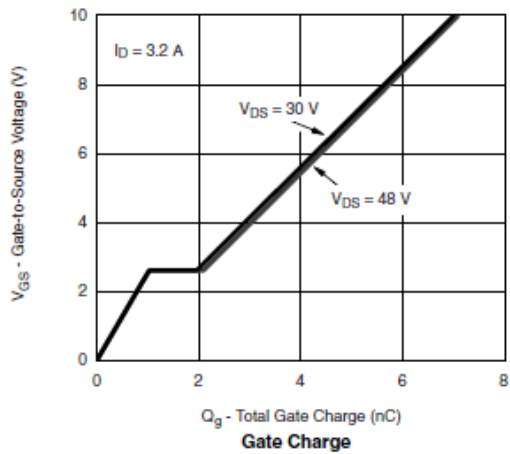
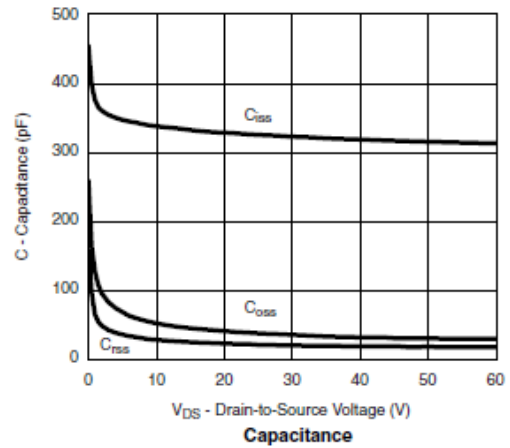
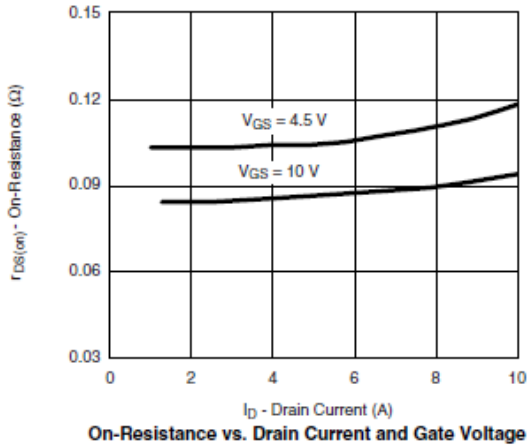
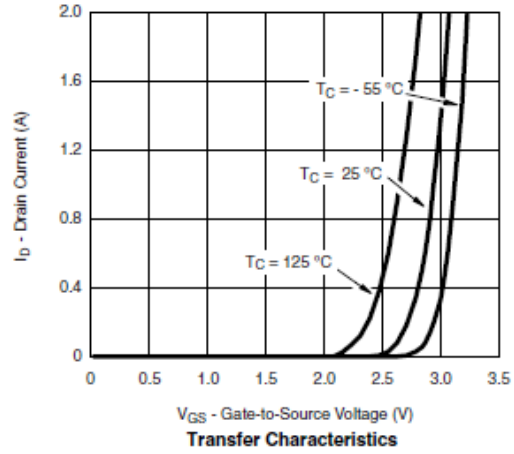
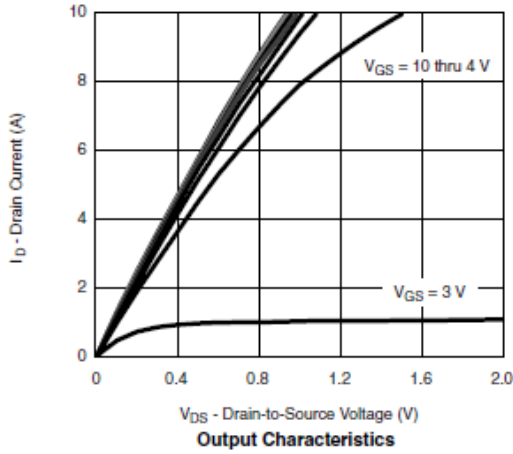
Electrical Characteristics

($T_A=25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu\text{A}$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.7		2.5	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$			1	uA
		$V_{DS}=60V, V_{GS}=0V$ $T_J=85^\circ\text{C}$			10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 5V, V_{GS}=10V$	10			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=8A$		128	140	m Ω
		$V_{GS}=4.5V, I_D=6A$		136	148	
Forward Transconductance	g_{FS}	$V_{DS}=15V, I_D=2.0A$		12		S
Diode Forward Voltage	V_{SD}	$I_S=2.0A, V_{GS}=0V$		0.85	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=30V, V_{GS}=10V$ $I_D \equiv 3A$		6	15	nC
Gate-Source Charge	Q_{gs}			1.5		
Gate-Drain Charge	Q_{gd}			2.0		
Input Capacitance	C_{iss}	$V_{DS}=35V, V_{GS}=0V$ $f=1\text{MHz}$		350		pF
Output Capacitance	C_{oss}			30		
Reverse Transfer Capacitance	C_{rss}			20		
Turn-On Time	$t_{d(on)}$	$V_{DD}=30V, R_L=10\Omega$ $I_D \equiv 5.0A, V_{GEN}=10V$ $R_G=3.0V$		6	12	ns
	t_r			6	12	
Turn-Off Time	$t_{d(off)}$			12	20	
	t_f			4	10	

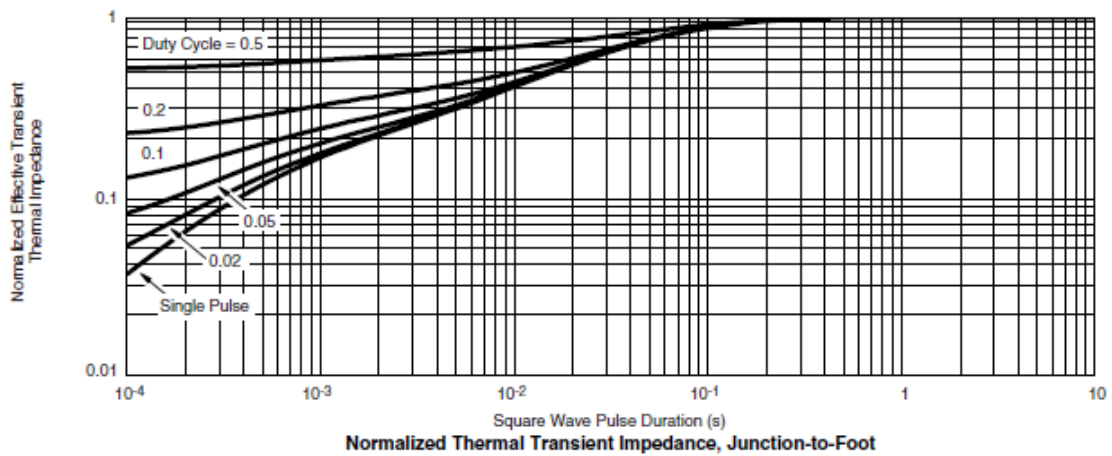
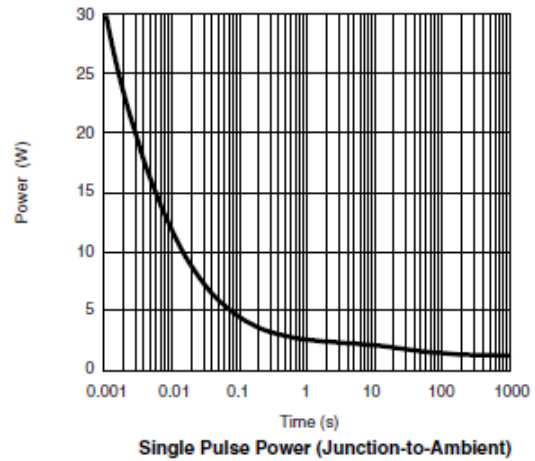
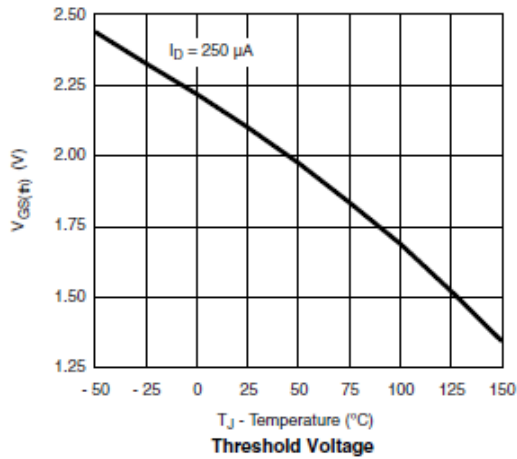
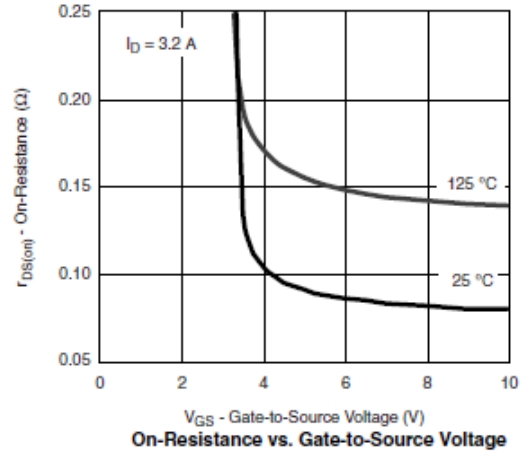
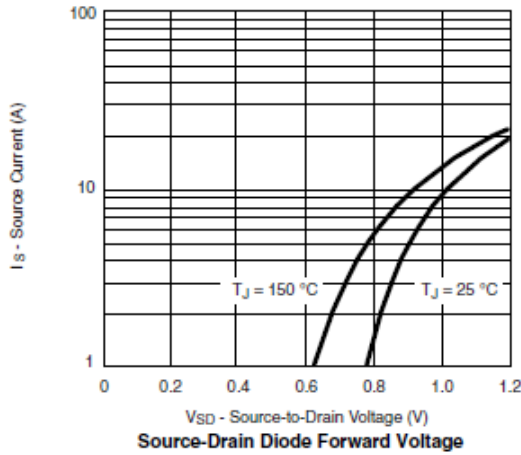


Typical Characteristics





Typical Characteristics





Typical Characteristics

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

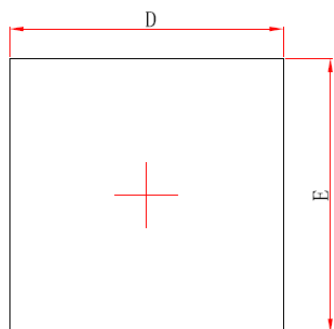


Unclamped Inductive Switching Test Circuit & Waveforms

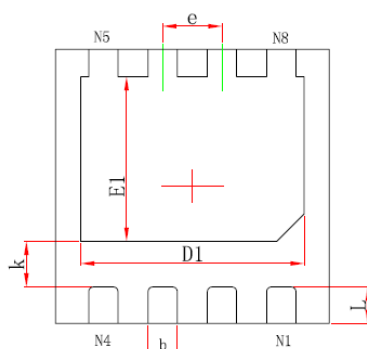




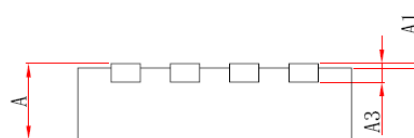
Package Information (DFN3X3-8L)



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	2.924	3.076	0.115	0.121
E	2.924	3.076	0.115	0.121
D1	2.350	2.550	0.093	0.100
E1	1.700	1.900	0.067	0.075
k	0.450	0.550	0.018	0.022
b	0.270	0.370	0.011	0.015
e	0.650TYP.		0.026TYP.	
L	0.324	0.476	0.013	0.019

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