



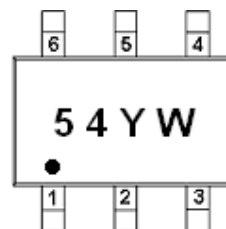
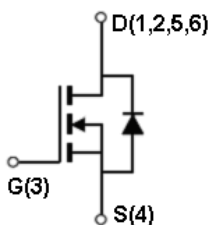
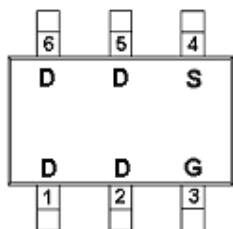
General Description

AFN3480, N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge. These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

Features

- 40V/5.6A, $R_{DS(ON)} = 54m\Omega @ V_{GS} = 10V$
- 40V/3.6A, $R_{DS(ON)} = 74m\Omega @ V_{GS} = 4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- TSOP-6 package design

Pin Description (TSOP-6)



Application

- Power Management in Note book
- LED Display
- DC-DC System
- LCD Panel

Pin Define

Pin	Symbol	Description
1	D	Drain
2	D	Drain
3	G	Gate
4	S	Source
5	D	Drain
6	D	Drain

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFN3454TS6RG	54YW	TSOP-6	Tape & Reel	3000 EA

- ※ 54 parts code
- ※ Y year code (0 ~ 9)
- ※ W week code (A ~ Z = 1 ~ 26 / a ~ z = 27 ~ 52)
- ※ AFN3454TS6RG : 7" Tape & Reel ; Pb- Free ; Halogen -Free



Absolute Maximum Ratings

($T_A=25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	40	V
Gate –Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current($T_J=150^\circ\text{C}$)	I_D	$T_A=25^\circ\text{C}$	5.6
		$T_A=70^\circ\text{C}$	3.6
Pulsed Drain Current	I_{DM}	15	A
Continuous Source Current(Diode Conduction)	I_S	1.7	A
Power Dissipation	P_D	$T_A=25^\circ\text{C}$	2.0
		$T_A=70^\circ\text{C}$	1.3
Operating Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55/150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	120	$^\circ\text{C/W}$

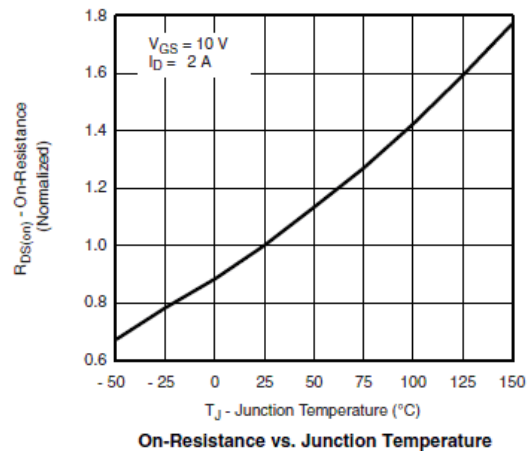
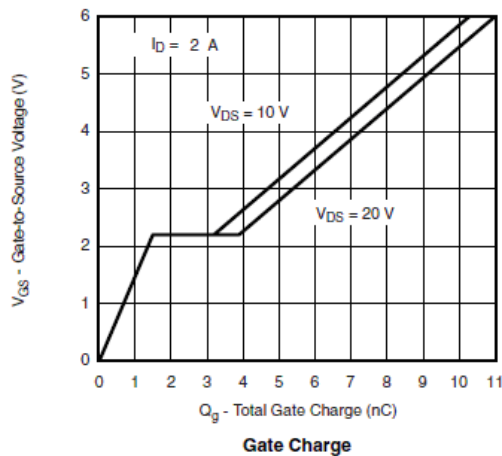
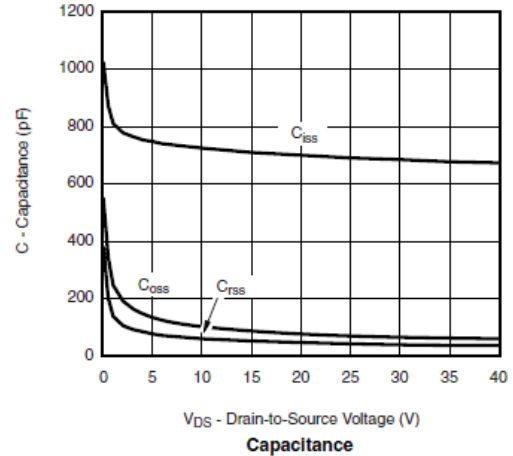
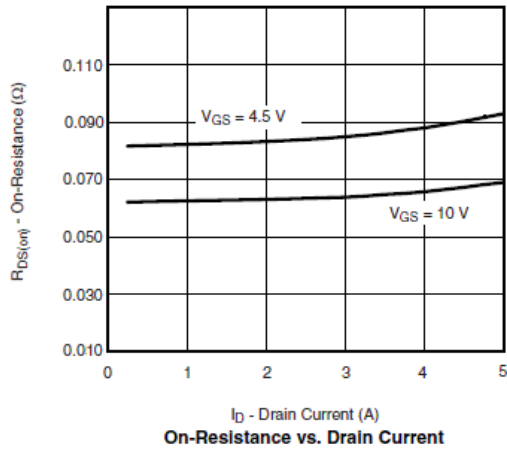
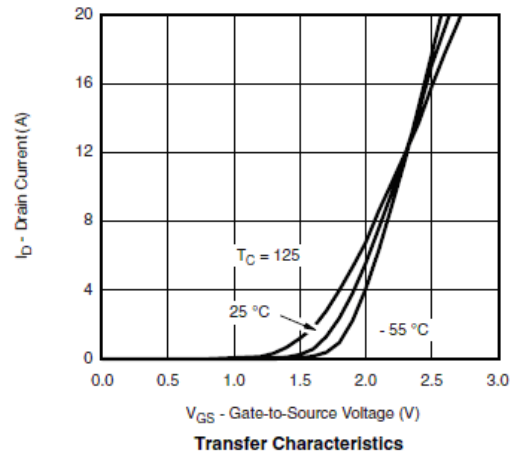
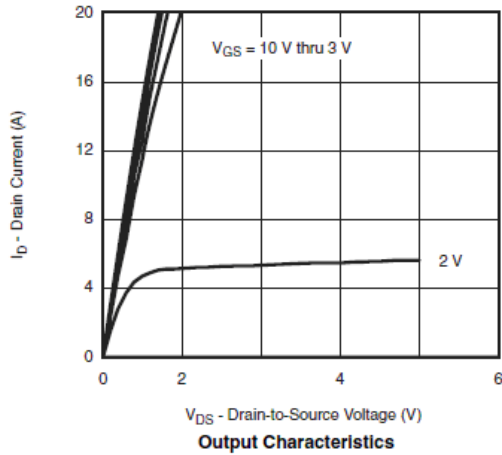
Electrical Characteristics

($T_A=25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu\text{A}$	40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.0		2.0	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V$			1	uA
		$V_{DS}=40V, V_{GS}=0V$ $T_J=85^\circ\text{C}$			10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 5V, V_{GS}=10V$	10			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=5.6A$		47	54	m Ω
		$V_{GS}=4.5V, I_D=3.6A$		66	74	
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=2.0A$		16		S
Diode Forward Voltage	V_{SD}	$I_S=1.5A, V_{GS}=0V$		0.85	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=20V, V_{GS}=4.5V$ $I_D \equiv 2A$		10	15	nC
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			2.5		
Input Capacitance	C_{iss}	$V_{DS}=20V, V_{GS}=0V$ $f=1\text{MHz}$		650		pF
Output Capacitance	C_{oss}			75		
Reverse Transfer Capacitance	C_{rss}			45		
Turn-On Time	$t_{d(on)}$	$V_{DD}=15V, R_L=15\Omega$ $I_D \equiv 1A, V_{GEN}=10V$ $R_G=6\Omega$		8	15	ns
	t_r			12	20	
Turn-Off Time	$t_{d(off)}$			28	40	
	t_f			8	15	

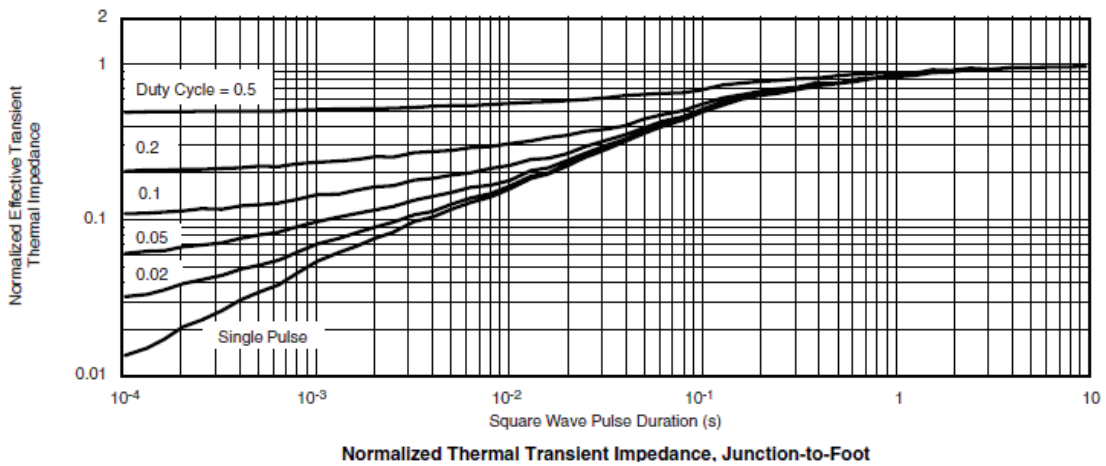
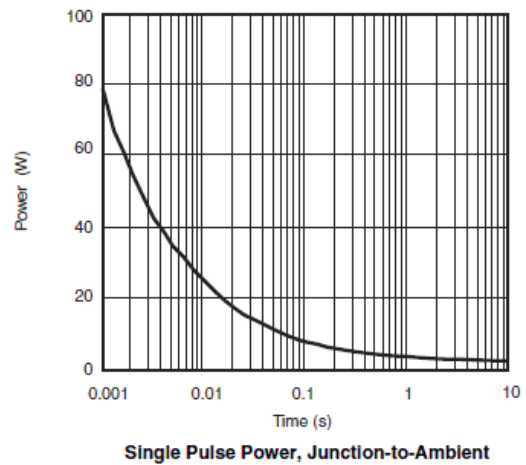
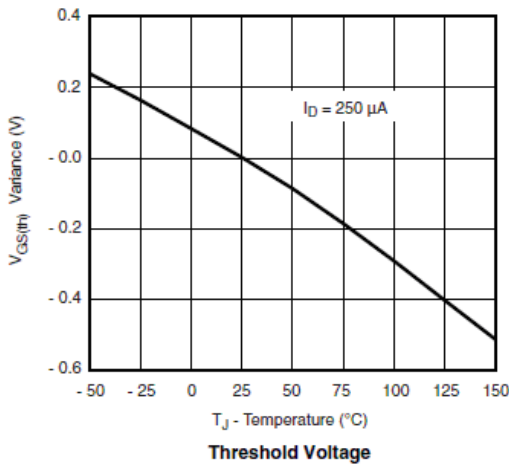
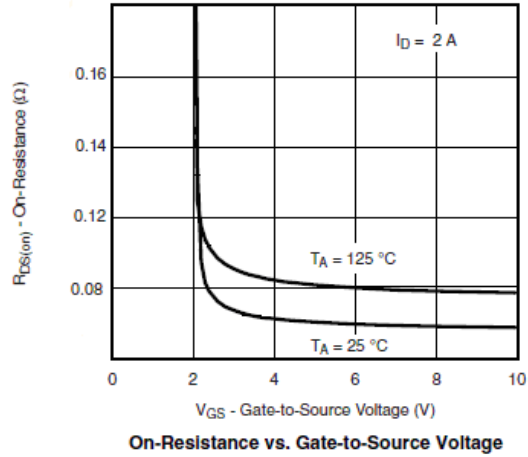
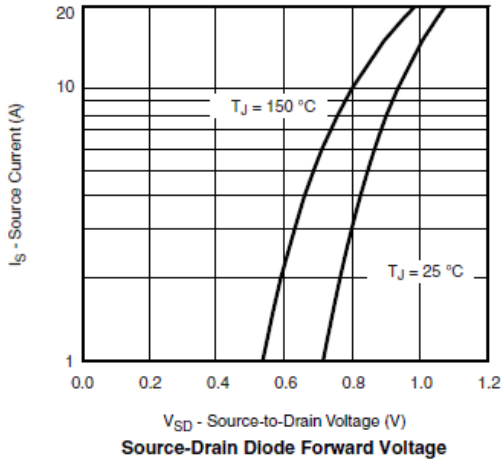


Typical Characteristics





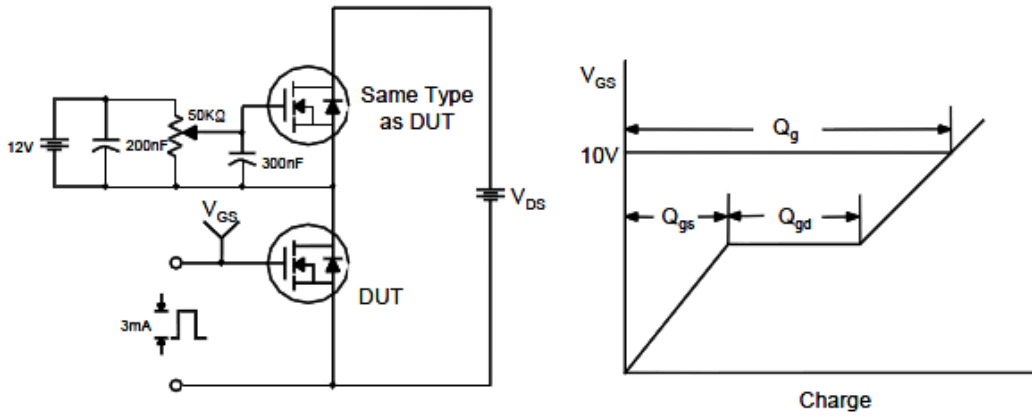
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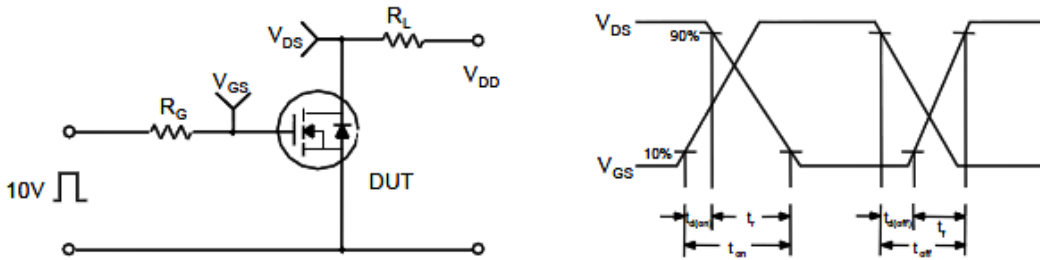


Typical Characteristics

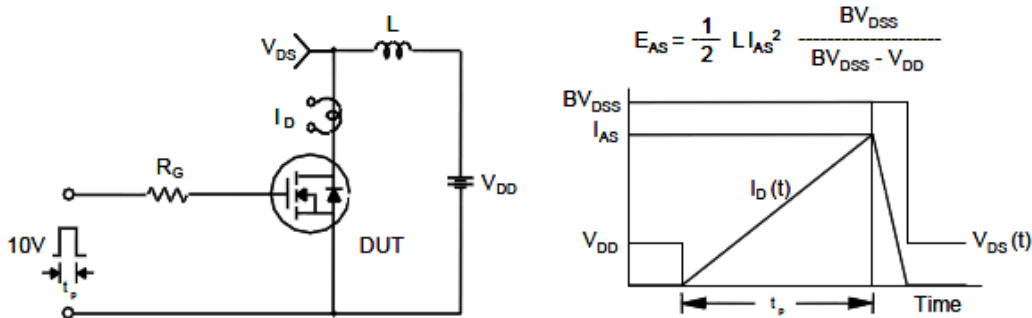
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

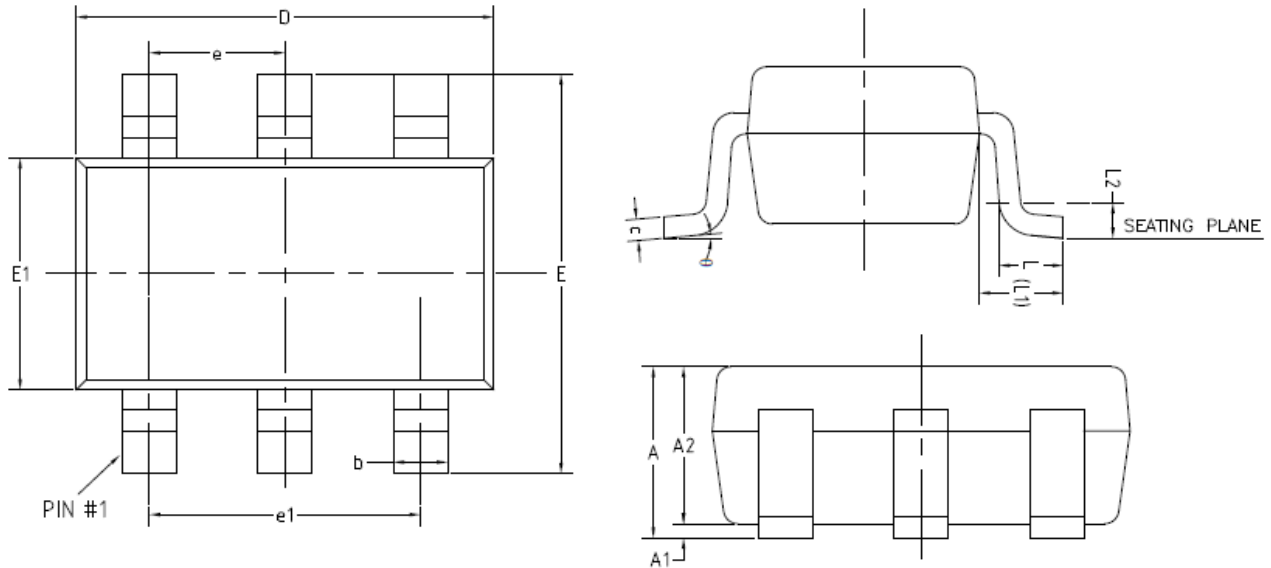


Unclamped Inductive Switching Test Circuit & Waveforms





Package Information (TSOP-6)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	—	0.90
A1	0	—	0.10
A2	0.70	0.75	0.80
b	0.35	—	0.50
c	0.08	—	0.20
D	2.82	2.92	3.02
E	2.65	2.80	2.95
E1	1.60	1.65	1.70
e	0.95(BSC)		
e1	1.90(BSC)		
L	0.30	0.45	0.60
L1	0.59REF		
L2	0.25BSC		
θ	0°	—	8°

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 2F, No.80, Sec.1, Cheng Kung Rd., Nan Kang Dist., Taipei City 115, Taiwan (R.O.C.)
 Tel : 886 2) 2651 3928
 Fax : 886 2) 2786 8483
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