



General Description

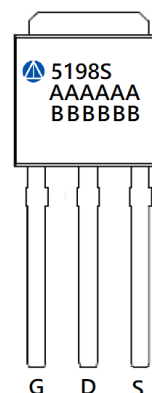
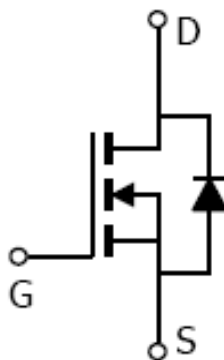
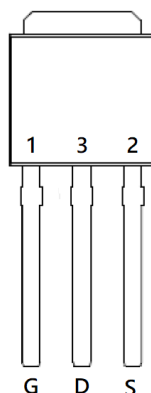
AFN5198S, N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

Features

- 150V/15A, $R_{DS(ON)} = 23m\Omega @ V_{GS} = 10V$
- 150V/10A, $R_{DS(ON)} = 26m\Omega @ V_{GS} = 6V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- TO-251-3L package design

Pin Description (TO-251-3L)



Application

- Primary Side Switch
- POL Synchronous buck converter
- LED Backlight for LCD TV

Pin Define

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFN5198ST251TG	5198S	TO-251-3L	Tube	80 EA

- ※ A Lot code
- ※ B Date code
- ※ AFN5198ST251TG : Tube ; Pb- Free ; Halogen –Free



Absolute Maximum Ratings($T_A=25^\circ\text{C}$ Unless otherwise noted)

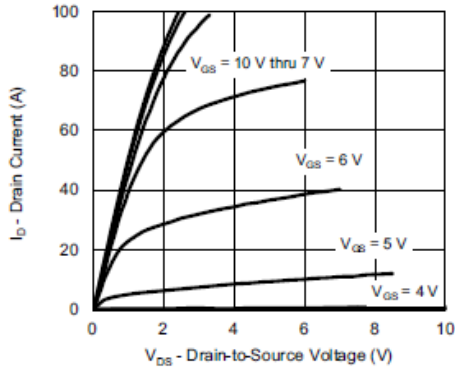
Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current($T_J=150^\circ\text{C}$)	I_{DSM}	$T_C=25^\circ\text{C}$	36
		$T_C=70^\circ\text{C}$	28
Pulsed Drain Current ($t=100\mu\text{s}$)	I_{DM}	$T_A=25^\circ\text{C}$	9.8
		$T_A=70^\circ\text{C}$	7.8
Continuous Source Current(Diode Conduction)	I_S	36	A
Single Pulse Avalanche Current	I_{AS}	$T_C=25^\circ\text{C}$	30
		$T_A=25^\circ\text{C}$	4.5
Power Dissipation	P_D	$L=0.1\text{mH}$	45
		$T_C=25^\circ\text{C}$	68
Operating Junction Temperature	T_J	$T_C=75^\circ\text{C}$	45
		$T_A=75^\circ\text{C}$	5.0
Storage Temperature Range	T_{STG}	-55/150	$^\circ\text{C}$
Maximum Junction-to-Ambient	$R_{\theta JA}$	25	$^\circ\text{C/W}$
Maximum Junction-to-Case (Drain)	$R_{\theta JA}$	1.8	

Electrical Characteristics($T_A=25^\circ\text{C}$ Unless otherwise noted)

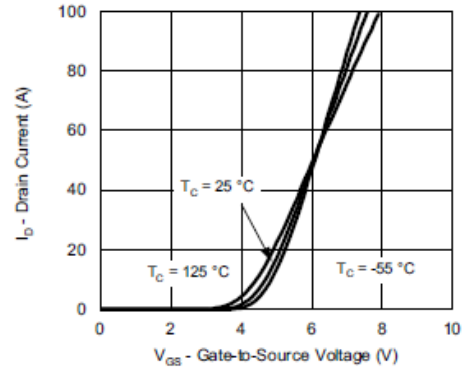
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu\text{A}$	150			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.0	3.0	4.0	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=120V, V_{GS}=0V$			1	uA
		$V_{DS}=120V, V_{GS}=0V$ $T_J=85^\circ\text{C}$			30	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 10V, V_{GS}=10V$	30			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=15A$		20	23	m Ω
		$V_{GS}=6V, I_D=10A$		22	26	
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=15A$		25		S
Diode Forward Voltage	V_{SD}	$I_S=8A, V_{GS}=0V$		0.75	1.3	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=75V, V_{GS}=7.5V$ $I_D=15A$		16	25	nC
Gate-Source Charge	Q_{gs}			5.5		
Gate-Drain Charge	Q_{gd}			6.8		
Gate Resistance	R_g	$f=1\text{MHz}$	0.3	1.0	2.0	Ω
Input Capacitance	C_{iss}	$V_{DS}=75V, V_{GS}=0V$ $f=1\text{MHz}$		1100		pF
Output Capacitance	C_{oss}			250		
Reverse Transfer Capacitance	C_{rss}			25		
Turn-On Time	$t_{d(on)}$	$V_{DD}=75V, R_L=5\Omega$ $I_D=15A, V_{GEN}=10V$ $R_G=1\Omega$		10	20	ns
	t_r			20	40	
Turn-Off Time	$t_{d(off)}$			15	30	
	t_f			10	20	



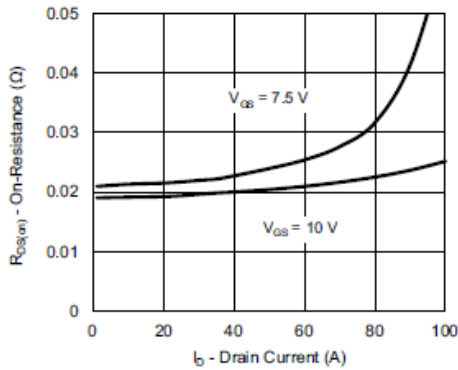
Typical Characteristics



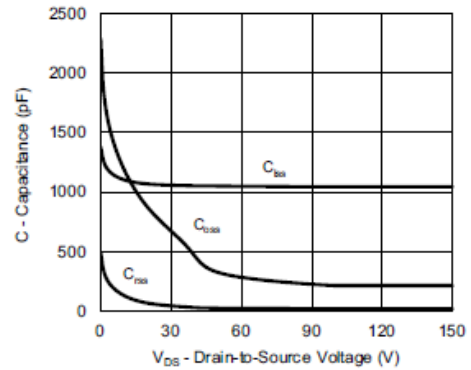
Output Characteristics



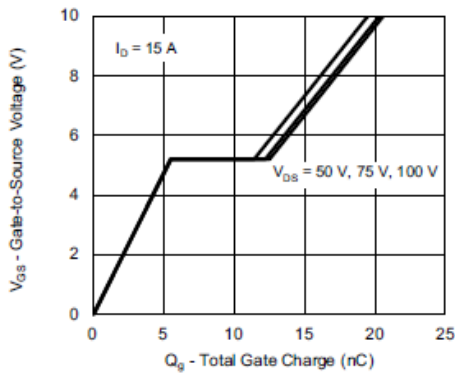
Transfer Characteristics



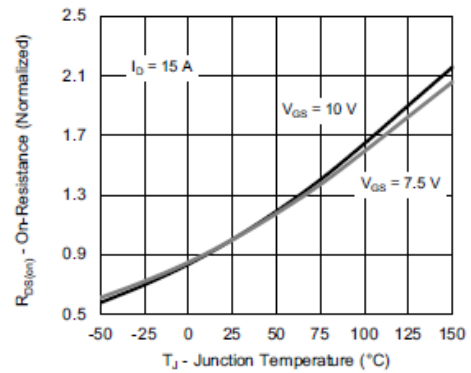
On-Resistance vs. Drain Current



Capacitance



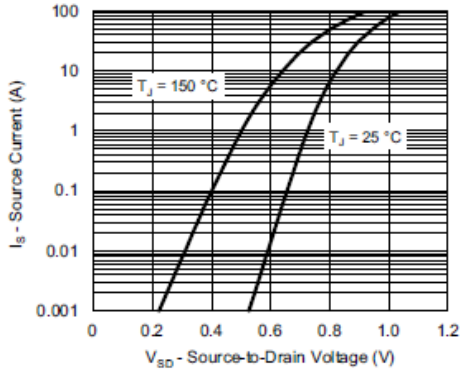
Gate Charge



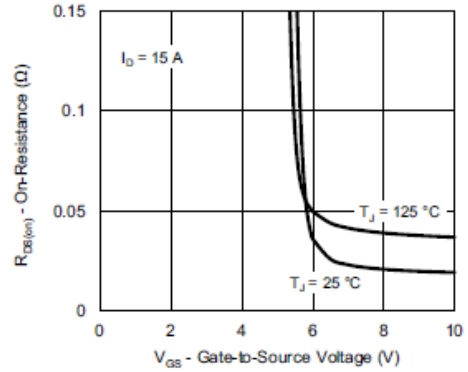
On-Resistance vs. Junction Temperature



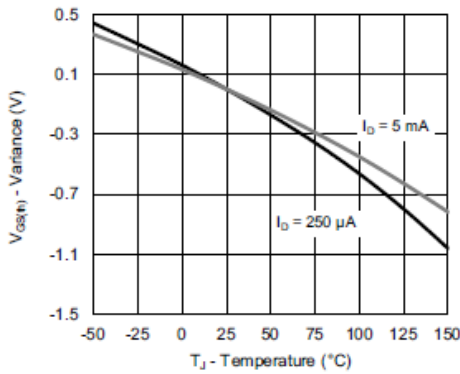
Typical Characteristics



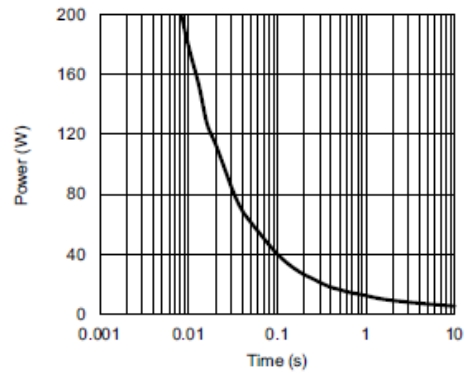
Source-Drain Diode Forward Voltage



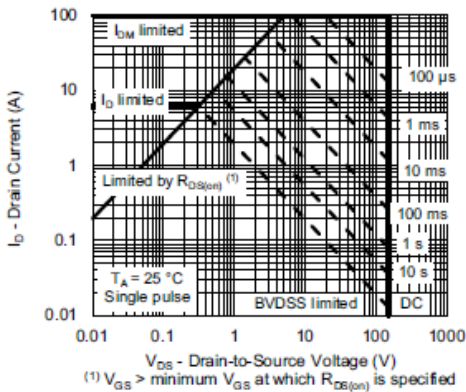
On-Resistance vs. Gate-to-Source Voltage



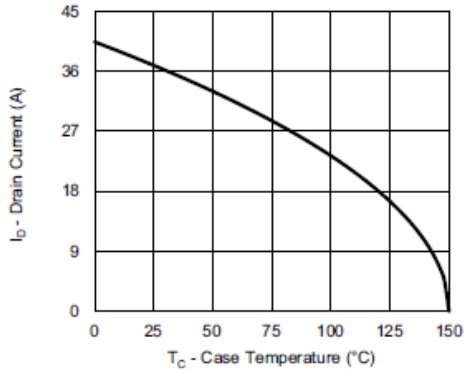
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



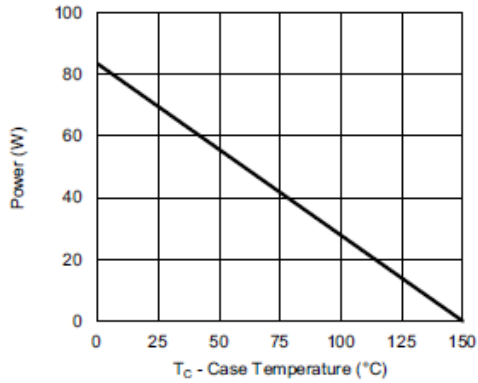
Safe Operating Area, Junction-to-Ambient



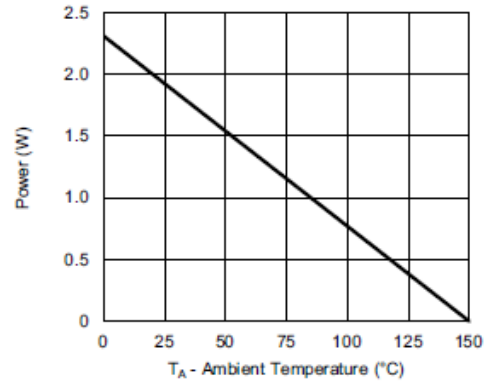
Current Derating ^a



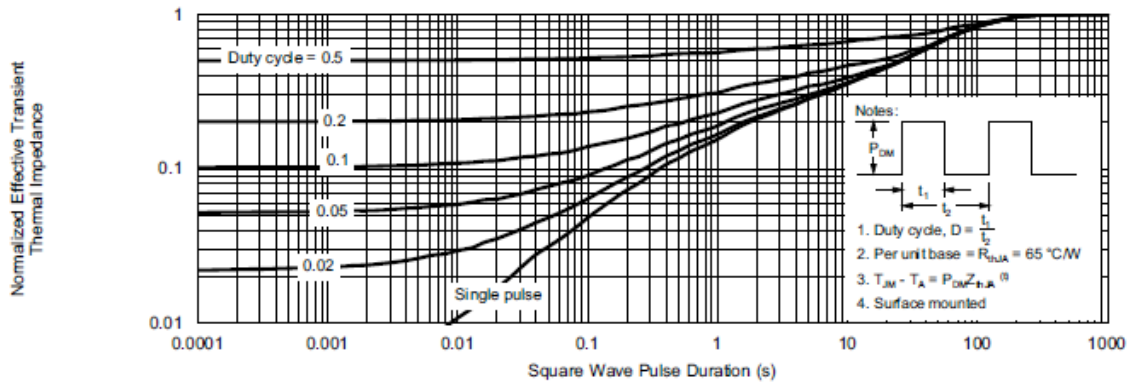
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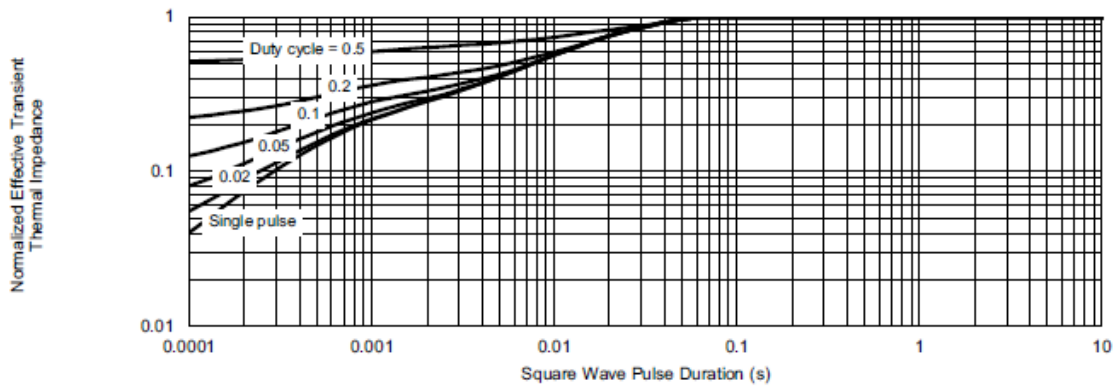
Power, Junction-to-Case



Power, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient

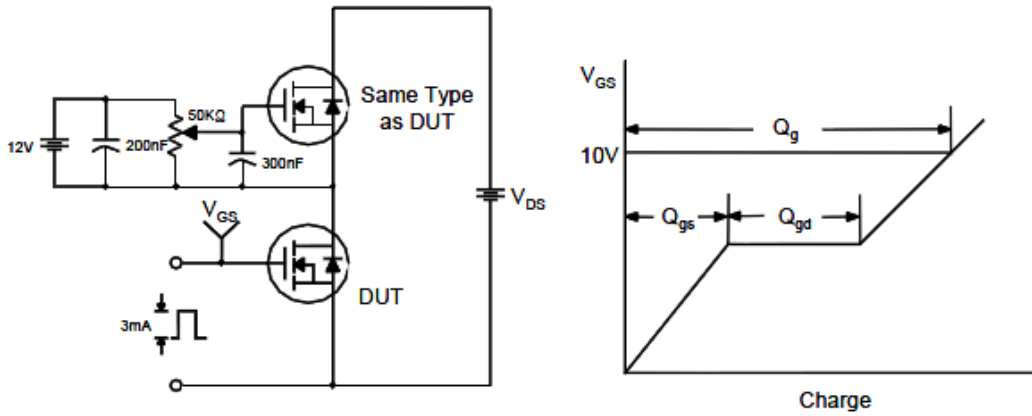


Normalized Thermal Transient Impedance, Junction-to-Case

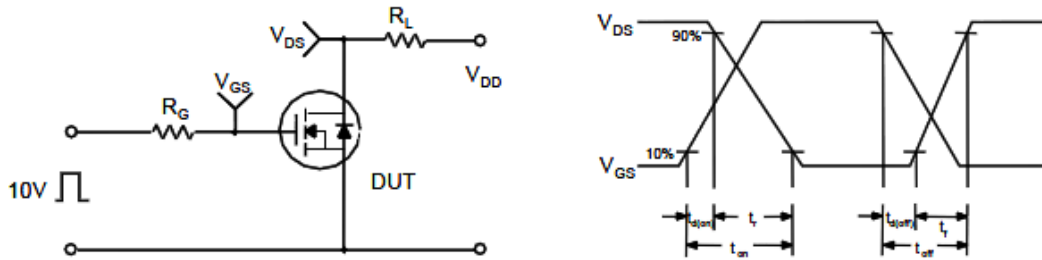


Typical Characteristics

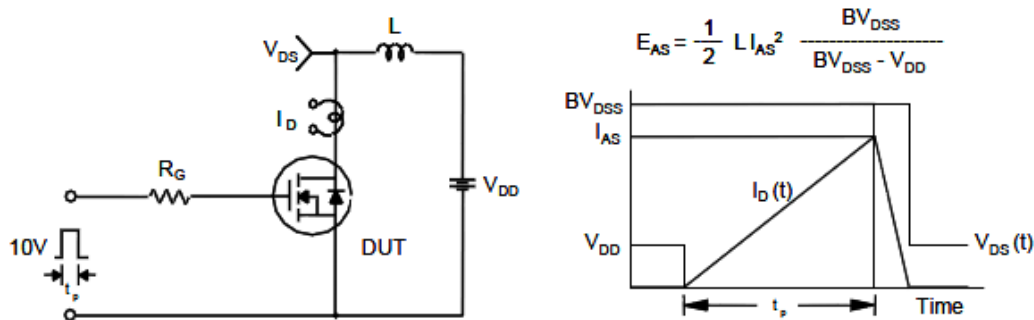
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

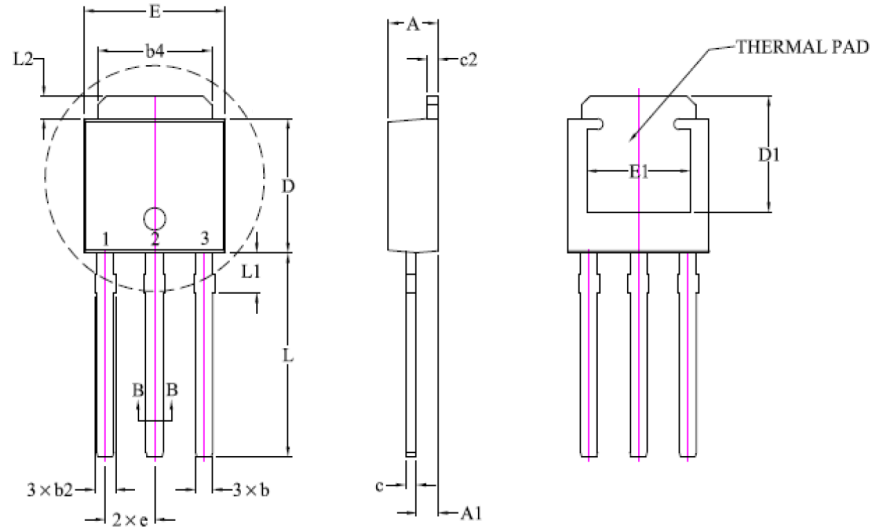


Unclamped Inductive Switching Test Circuit & Waveforms





Package Information (TO-251-3L)



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.220	2.420	0.087	0.095
A1	0.890	1.140	0.035	0.045
b	0.550	0.670	0.022	0.026
b1	0.550	0.650	0.022	0.025
b2	0.760	0.960	0.030	0.038
b4	5.200	5.400	0.205	0.213
c	0.460	0.570	0.018	0.023
c1	0.450	0.550	0.018	0.022
c2	0.450	0.550	0.018	0.022
D	5.950	6.250	0.234	0.246
D1	4.200	4.500	0.165	0.177
E	6.400	6.700	0.252	0.264
E1	4.750	4.850	0.187	0.191
e	2.28 REF		0.090 REF	
L	8.900	9.500	0.350	0.374
L1	1.900	2.290	0.075	0.090
L2	0.900	1.000	0.035	0.039

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