



General Description

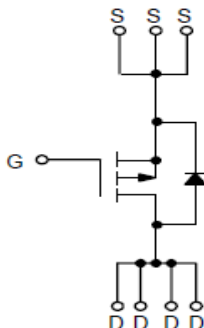
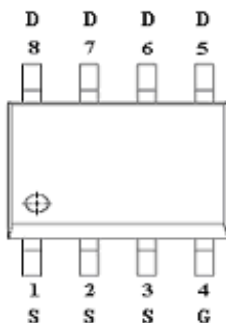
AFP1810, P-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

Features

- $I_D = -2.0A, R_{DS(ON)} = 235m\Omega @ V_{GS} = -10V$
- $I_D = -1.0A, R_{DS(ON)} = 245m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- SOP-8P package design

Pin Description (SOP-8P)



Application

- Full Bridge DC/DC Converter
- Load Switch

Pin Define

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFP1810S8RG	1810	SOP-8P	Tape & Reel	3000 EA

※ A Lot code

※ B Date code

※ AFP1810S8RG : 13" Tape & Reel ; Pb- Free ; Halogen -Free



Absolute Maximum Ratings

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	-100	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	I _D	T _A =25°C	-2.5
		T _A =70°C	-2.0
Pulsed Drain Current	I _{DM}	-10	A
Continuous Source Current(Diode Conduction)	I _S	-2	A
Power Dissipation	P _D	T _A =25°C	2.8
		T _A =70°C	1.8
Operating Junction Temperature	T _J	150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	62.5	°C/W

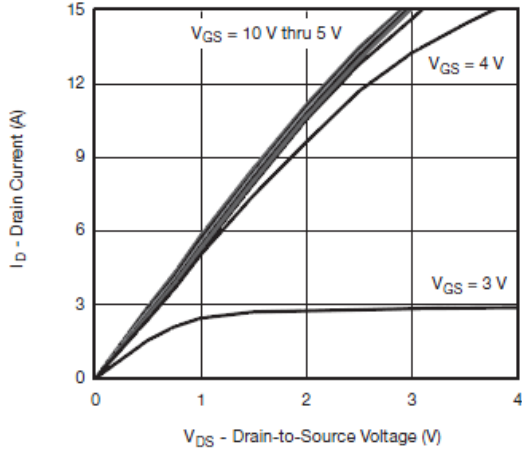
Electrical Characteristics

(T_A=25°C Unless otherwise noted)

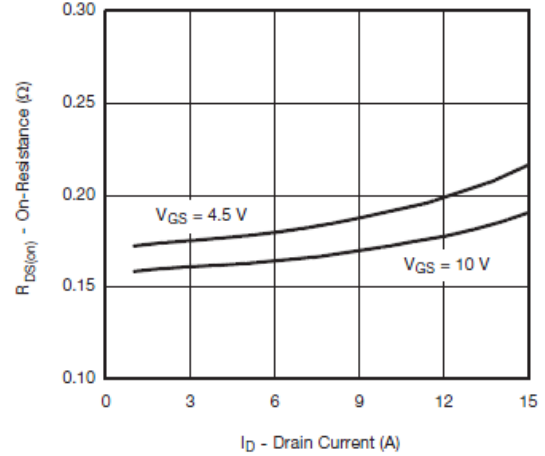
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D = -250uA	-100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D = -250uA	-1.0		-2.5	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -80V, V _{GS} =0V			-1	uA
		V _{DS} = -80V, V _{GS} =0V T _J =85°C			-30	
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = -10V, I _D =-2.0A		210	235	mΩ
		V _{GS} = -4.5V, I _D =-1.0A		220	245	
Forward Transconductance	g _{FS}	V _{DS} = -15V, I _D = -2.0A		9		S
Diode Forward Voltage	V _{SD}	I _S = -2A, V _{GS} =0V		-0.8	-1.3	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =-50V, V _{GS} =-4.5V I _D = -2.0A		12	20	nC
Gate-Source Charge	Q _{gs}			3.0		
Gate-Drain Charge	Q _{gd}			4.5		
Input Capacitance	C _{iss}	V _{DS} =-25V, V _{GS} =0V f=1MHz		1300		pF
Output Capacitance	C _{oss}			100		
Reverse Transfer Capacitance	C _{rss}			60		
Turn-On Time	t _{d(on)}	V _{DD} =-50V, R _L =10Ω I _D ≡-1.0A, V _{GEN} =-10V R _G =1Ω		8	15	ns
	t _r			15	20	
Turn-Off Time	t _{d(off)}			35	50	
	t _f			10	25	



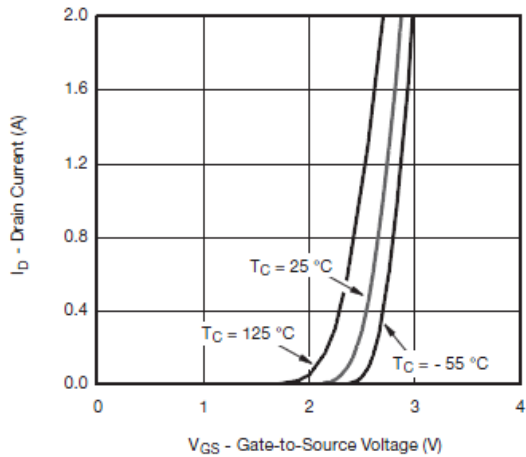
Typical Characteristics



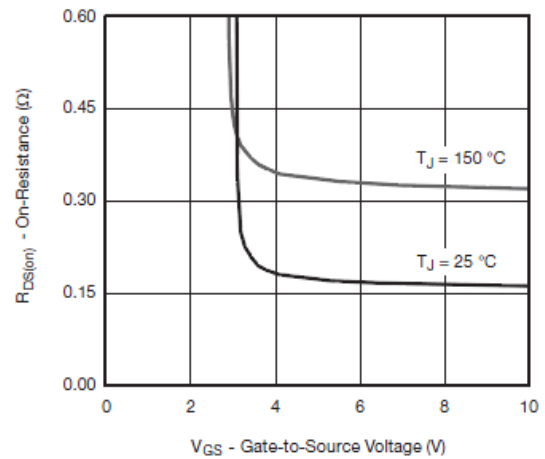
Output Characteristics



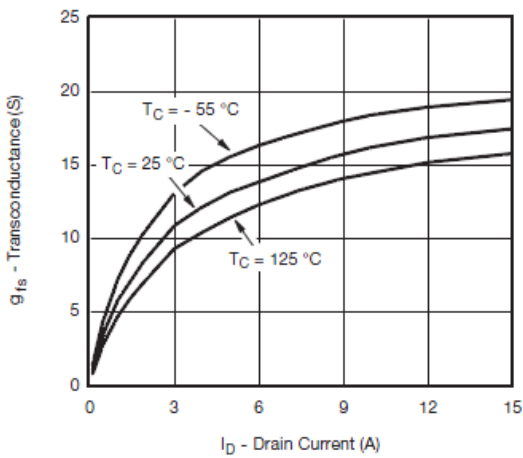
On-Resistance vs. Drain Current



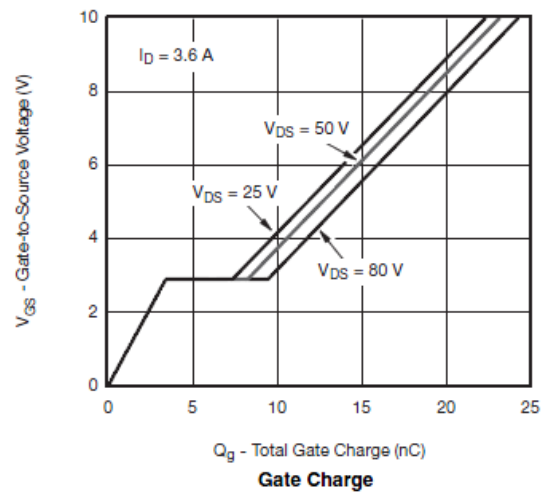
Transfer Characteristics



On-Resistance vs. Gate-to-Source Voltage



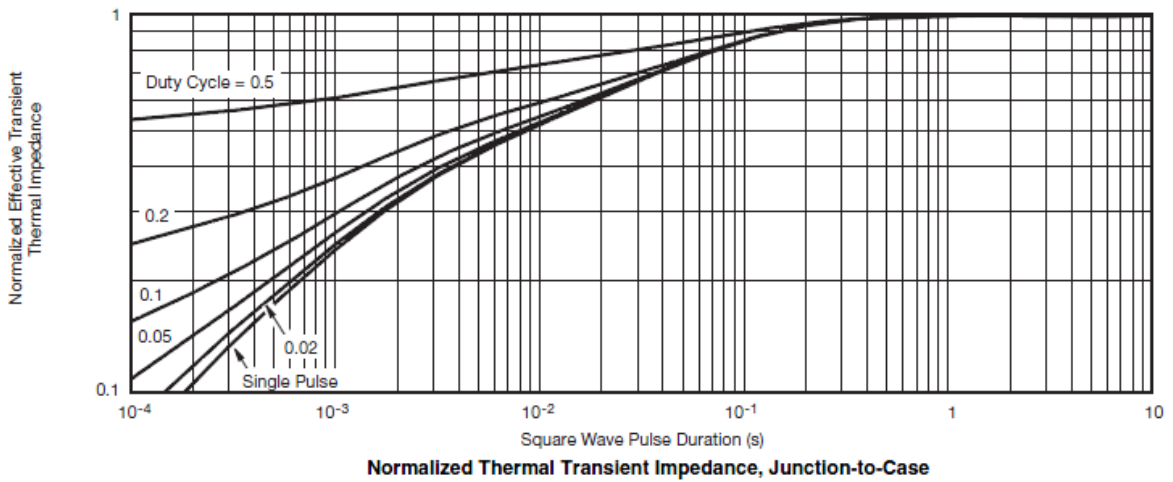
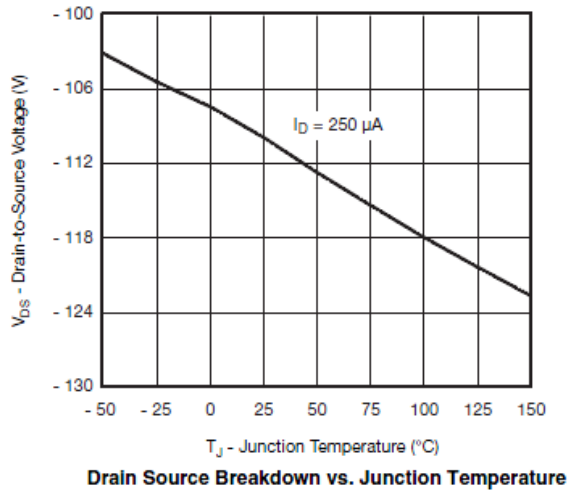
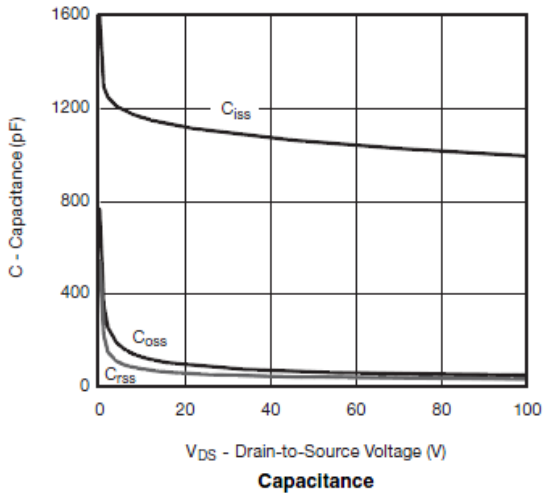
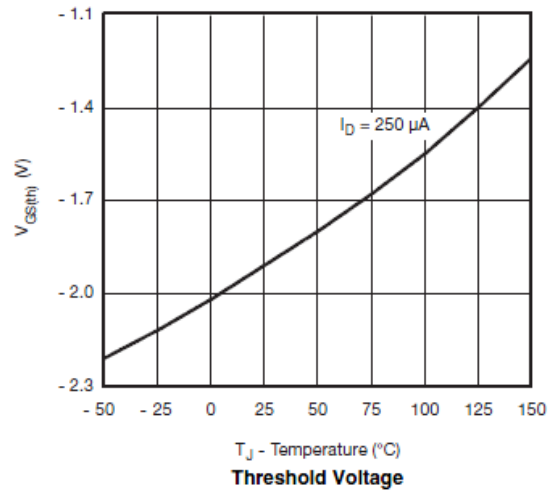
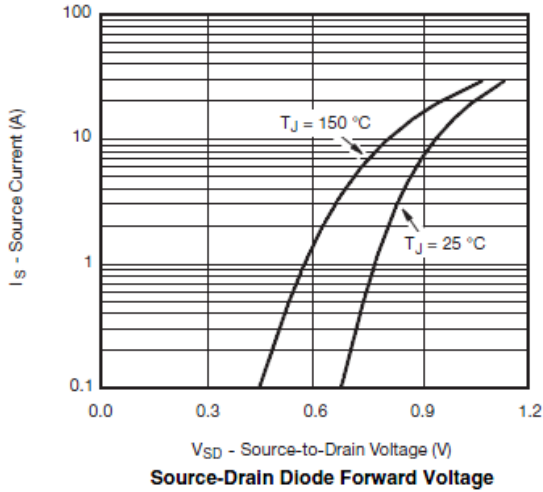
Transconductance



Gate Charge



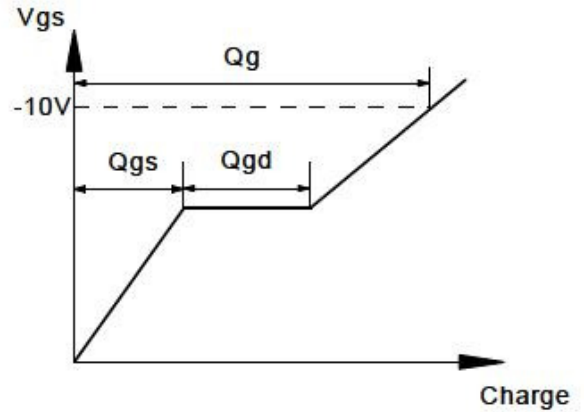
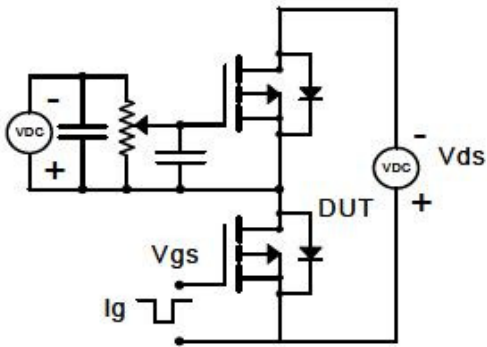
Typical Characteristics



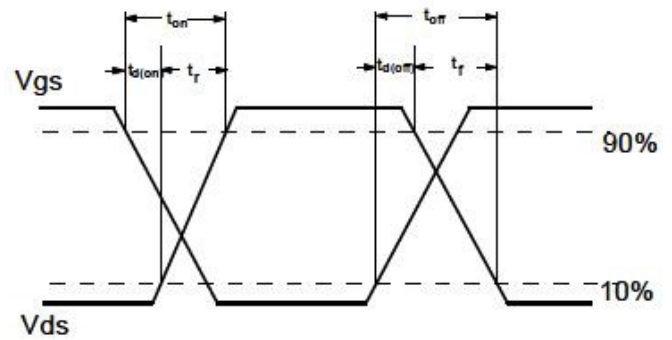
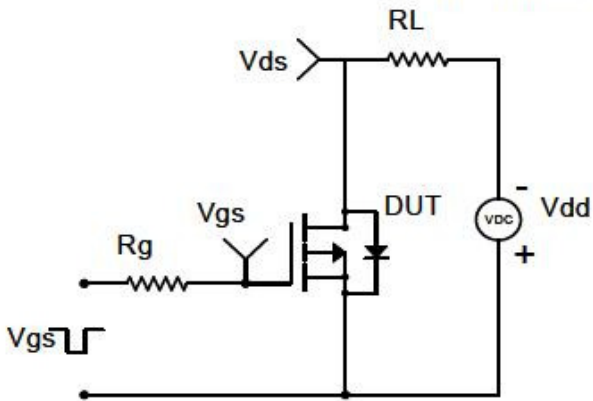


Typical Characteristics

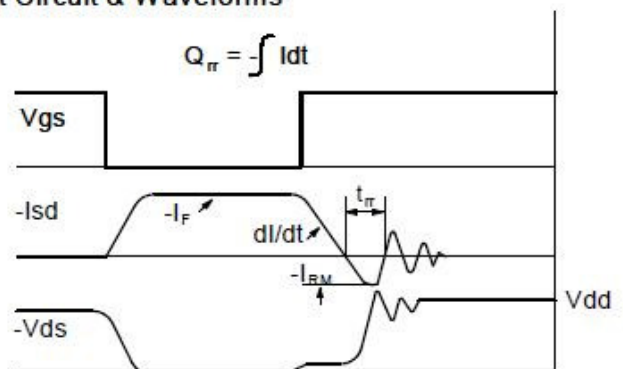
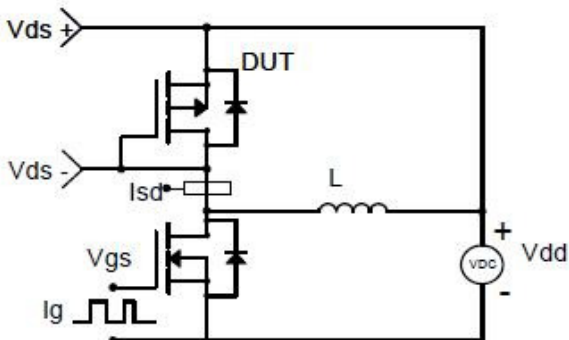
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

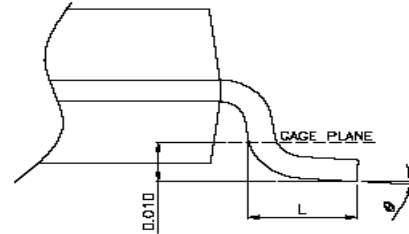
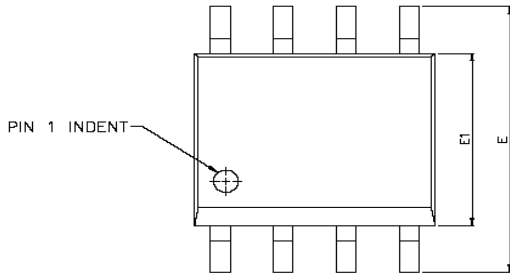


Diode Recovery Test Circuit & Waveforms

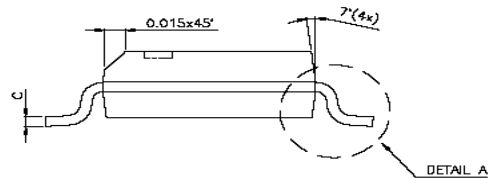
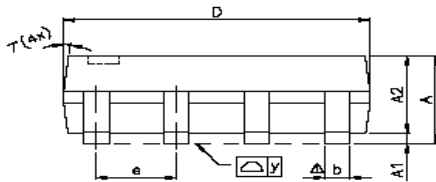




Package Information (SOP-8P)



DETAIL A



DETAIL A

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
Δ y	—	—	0.076	—	—	0.003
θ	0°	—	8°	0°	—	8°

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