Alfa-MOS Technology

AFP6679S
30V P-Channel Enhancement Mode MOSFET

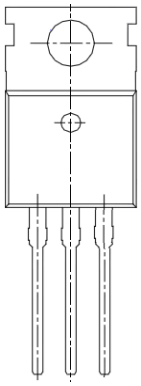
General Description

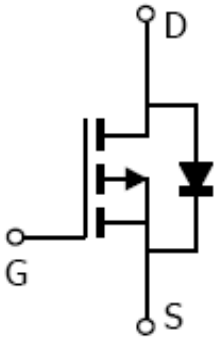
AFP6679S, P-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.
These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

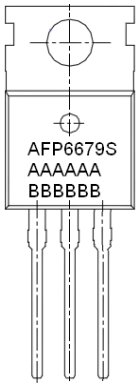
Features

- -30V/-20A,$R_{DS(ON)}$= 9.8mΩ@V_{GS}=-10V
- -30V/-15A,$R_{DS(ON)}$=14mΩ@V_{GS}=-4.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- TO-220-3L package design

Pin Description (TO-220-3L)







Application

- Power Switch
- Load switch in high current applications
- DC/DC converters

Pin Define

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFP6679ST220TG	AFP6679S AAAAAA BBBBBB	TO-220-3L	Tube	50 EA

※ A Lot code
※ B Date code
※ AFP6679ST220TG : Tube ; Pb- Free ; Halogen- Free

Absolute Maximum Ratings

(T_A=25℃ Unless otherwise noted)

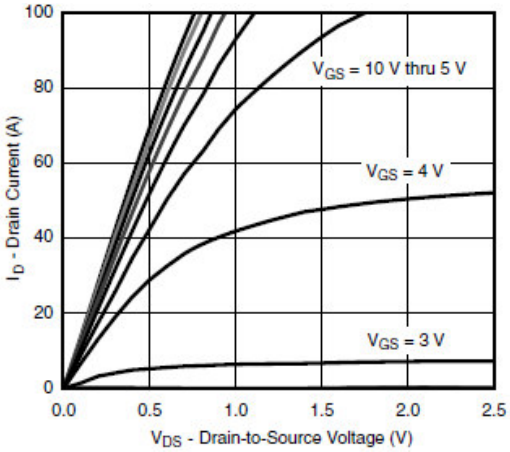
Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-30	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_C=25℃	I_D	-45.0	A
	T_C=70℃		-45.0	
Pulsed Drain Current		I_{DM}	-100	A
Avalanche Current	L=0.1 mH	I_{AS}	-35	A
Single Avalanche Energy		E_{AS}	61	mJ
Power Dissipation	T_C=25℃	P_D	75	W
Operating Junction Temperature		T_J	150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	62.5	℃/W

Electrical Characteristics

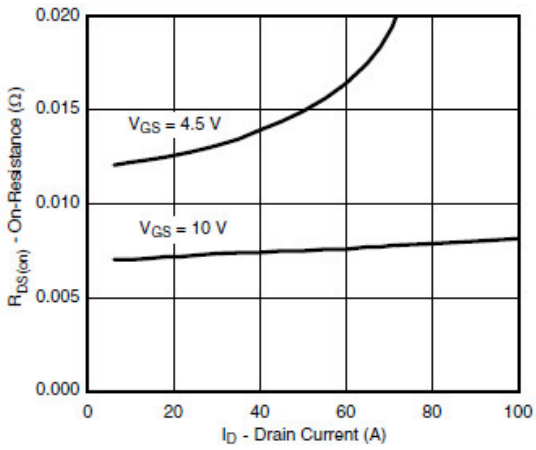
(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-1.0		-3.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-24V,V_{GS}=0V			-1	uA
		V_{DS}=-24V,V_{GS}=0V T_A=85℃			-30	
On-State Drain Current	$I_{D(on)}$	V_{DS}≦-10V,V_{GS}=-10V	-50			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10.0V,I_D=-20A		8.8	9.8	mΩ
		V_{GS}=-4.5V,I_D=-15A		12.5	14	
Forward Transconductance	g_{FS}	V_{DS}=-15V,I_D=-20A		45		S
Diode Forward Voltage	V_{SD}	I_S=-10A,V_{GS}=0V		-0.7	-1.3	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-15V,V_{GS}=-10V I_D≡-20A		60	90	nC
Gate-Source Charge	Q_{gs}			10		
Gate-Drain Charge	Q_{gd}			15		
Input Capacitance	C_{iss}	V_{DS}=-15V,V_{GS}=0V f=1MHz		2750		pF
Output Capacitance	C_{oss}			515		
Reverse Transfer Capacitance	C_{rss}			445		
Turn-On Time	$t_{d(on)}$	V_{DD}=-15V,R_L=1.5Ω I_D≡-10A,V_{GEN}=-10V R_G=1Ω		12	20	ns
	t_r			11	20	
Turn-Off Time	$t_{d(off)}$			40	60	
	t_f			12	20	

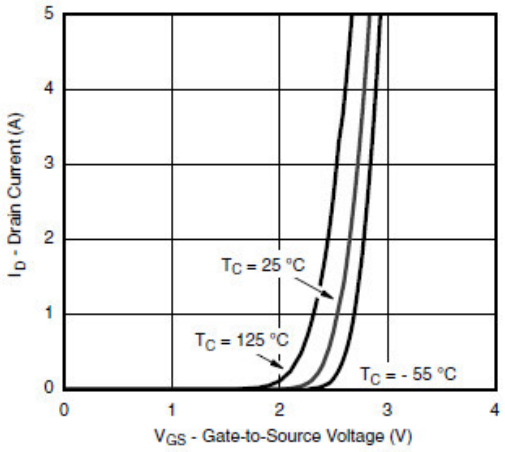
Typical Characteristics



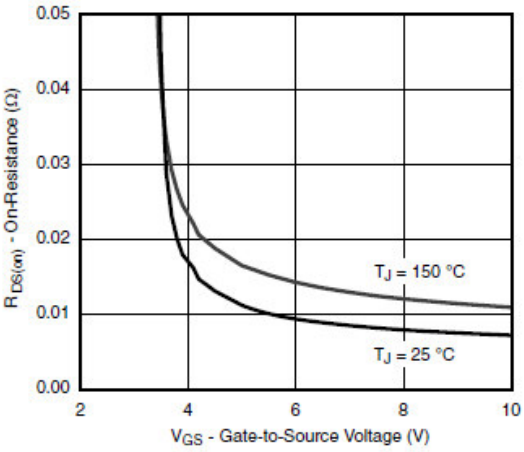
Output Characteristics



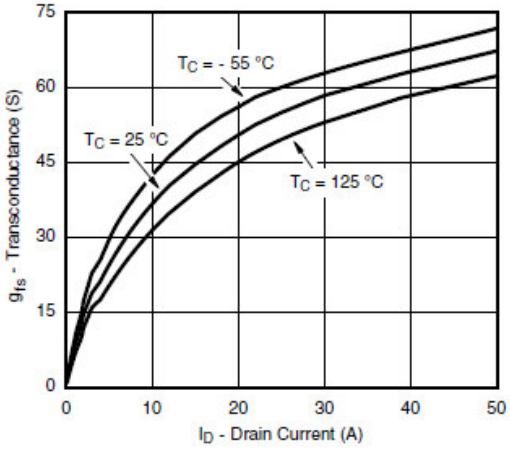
On-Resistance vs. Drain Current

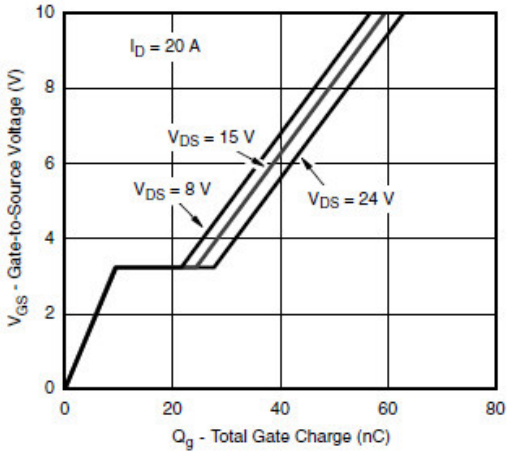


Transfer Characteristic

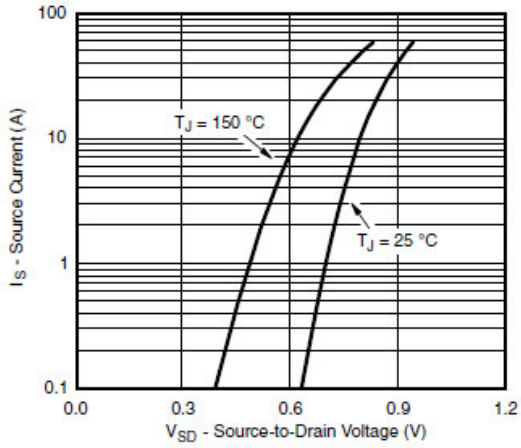


On-Resistance vs. Gate-to-Source Voltage

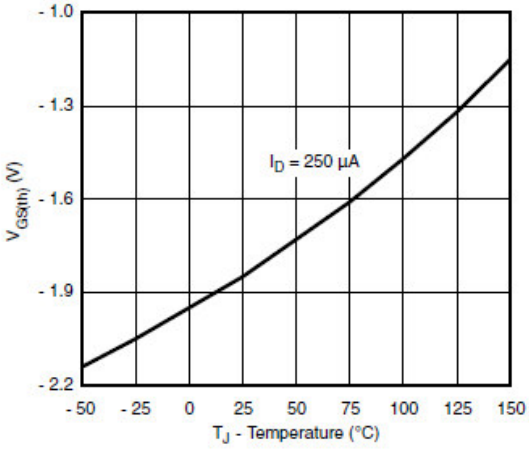




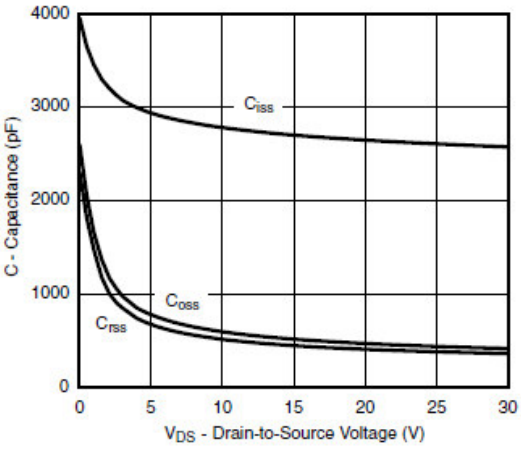
Typical Characteristics



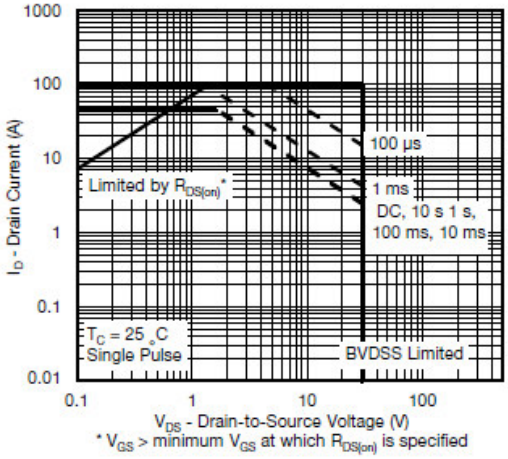
Source-Drain Diode Forward Voltage



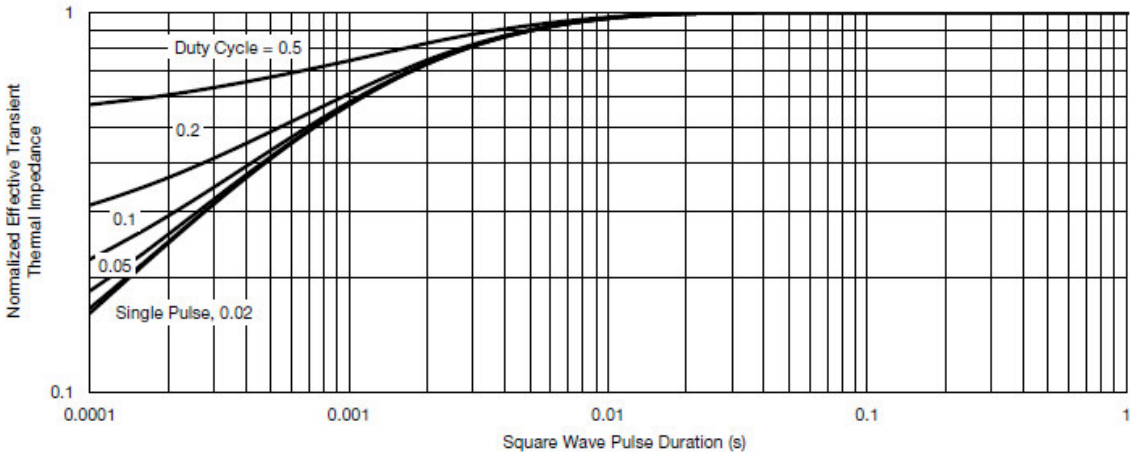
Threshold Voltage



Capacitance

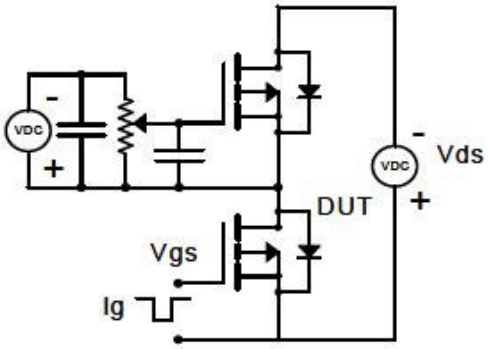


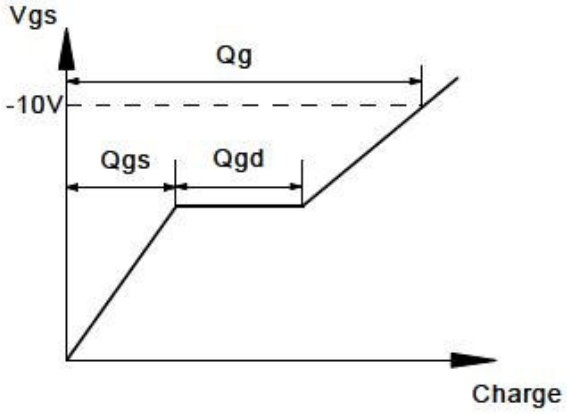
Safe Operating Area



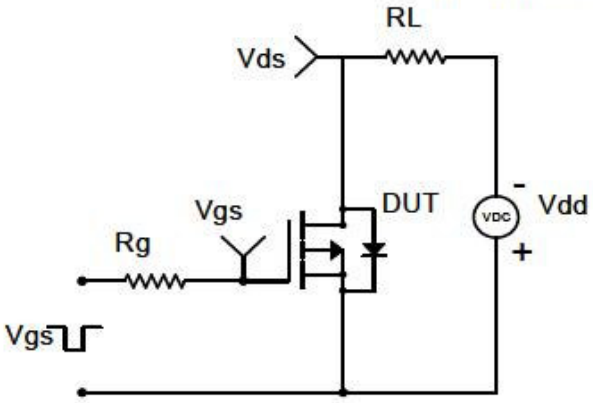
Typical Characteristics

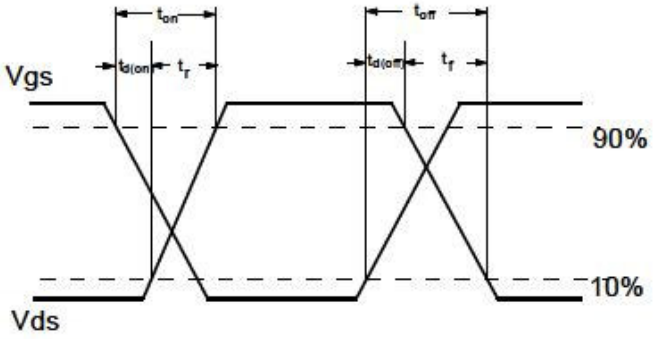
Gate Charge Test Circuit & Waveform



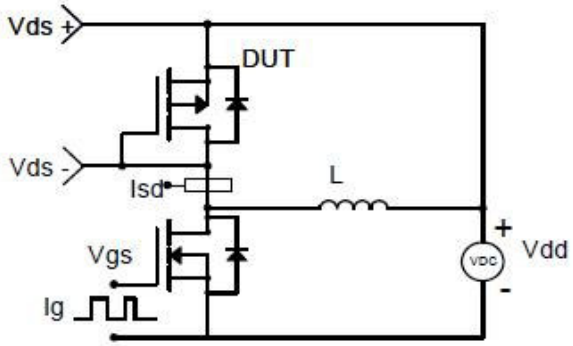


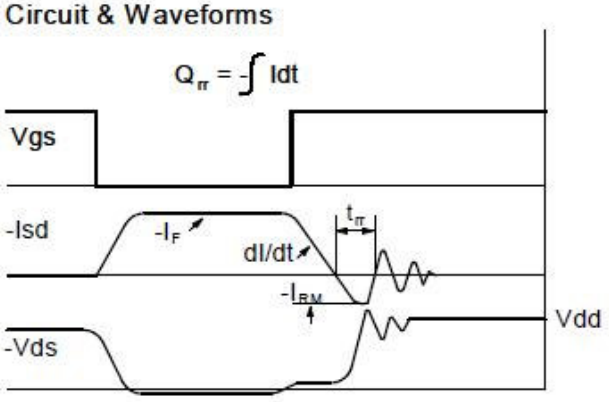
Resistive Switching Test Circuit & Waveforms



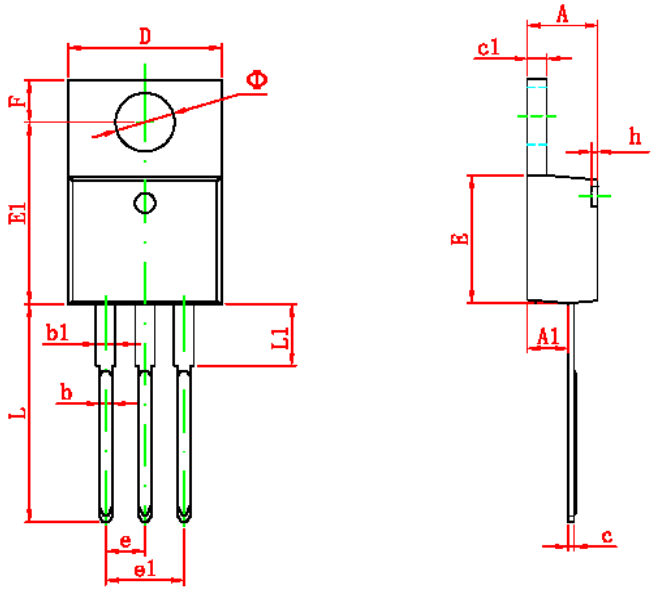


Diode Recovery Test Circuit & Waveforms





Package Information (TO-220-3L)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.470	4.670	0.176	0.184
A1	2.520	2.820	0.099	0.111
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
E	8.500	8.900	0.335	0.350
E1	12.060	12.460	0.475	0.491
e	2.540 TYP		0.100 TYP	
e1	4.980	5.180	0.196	0.204
F	2.590	2.890	0.102	0.114
h	0.000	0.300	0.000	0.012
L	13.400	13.800	0.528	0.543
L1	3.560	3.960	0.140	0.156
• •	3.735	3.935	0.147	0.155

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