



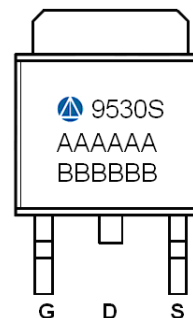
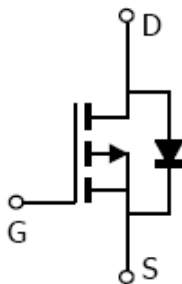
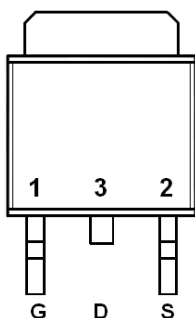
General Description

AFP9530S, P-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge. These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

Features

- -60V/-25A, $R_{DS(ON)} = 26m\Omega @ V_{GS} = -10V$
- -60V/-15A, $R_{DS(ON)} = 36m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- TO-252-2L package design

Pin Description (TO-252-2L)



Application

- Load Switches
- Half-Bridge Motor Drives
- High Voltage Non-Synchronous Buck Converters

Pin Define

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFP9530ST252RG	9530S	TO-252-2L	Tape & Reel	2500 EA

- ※ A Lot code
- ※ B Date code
- ※ AFP9530ST252RG : 13" Tape & Reel ; Pb- Free ; Halogen -Free



Absolute Maximum Ratings

($T_A=25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-60	V
Gate-Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current ($T_J=150^\circ\text{C}$)	I_D	$T_c=25^\circ\text{C}$	-35
		$T_c=70^\circ\text{C}$	-20
Pulsed Drain Current	I_{DM}	-25	A
Continuous Source-Drain Diode Current	I_S	-6	A
Power Dissipation	P_D	$T_A=25^\circ\text{C}$	40
		$T_A=70^\circ\text{C}$	15
Operating Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55/150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

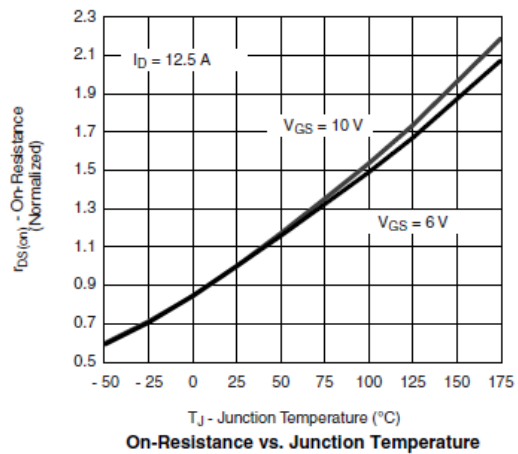
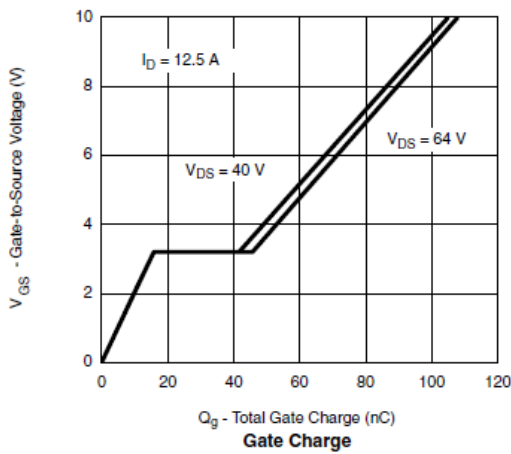
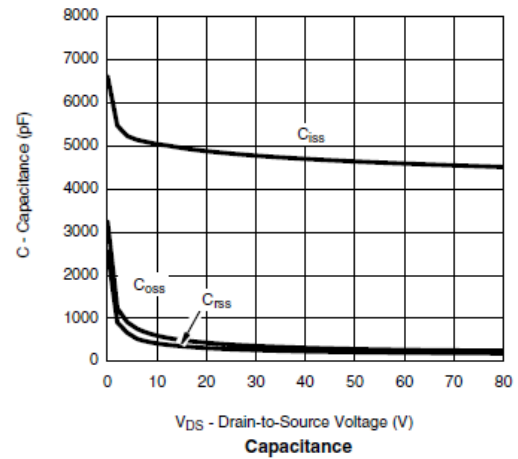
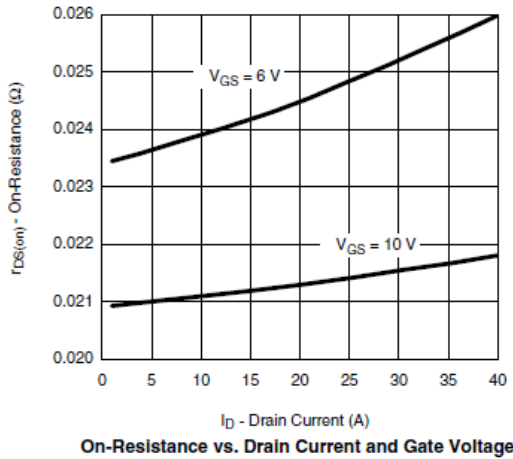
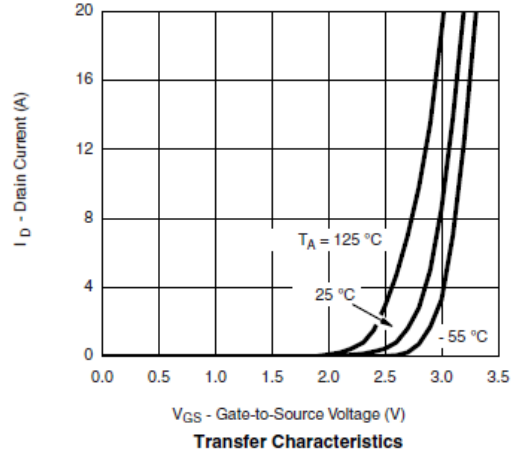
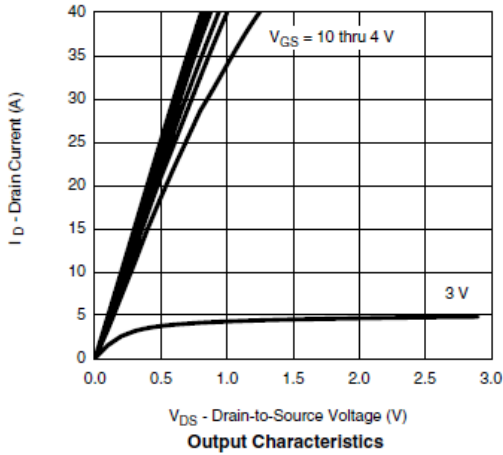
Electrical Characteristics

($T_A=25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu\text{A}$	-60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-1.0		-2.0	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-48V, V_{GS}=0V$			-1	uA
		$V_{DS}=-48V, V_{GS}=0V$ $T_J=85^\circ\text{C}$			-20	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq -5V, V_{GS}=-10V$	-10			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-25A$		20	26	m Ω
		$V_{GS}=-4.5V, I_D=-15A$		28	36	
Forward Transconductance	g_{FS}	$V_{DS}=-15V, I_D=-15A$		45		S
Diode Forward Voltage	V_{SD}	$I_S=-3A, V_{GS}=0V$		-0.8	-1.3	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-30V, V_{GS}=-4.5V$ $I_D=-15.0A$		50	95	nC
Gate-Source Charge	Q_{gs}			15		
Gate-Drain Charge	Q_{gd}			25		
Input Capacitance	C_{iss}	$V_{DS}=-30V, V_{GS}=0V$ $f=1\text{MHz}$		4200		pF
Output Capacitance	C_{oss}			300		
Reverse Transfer Capacitance	C_{rss}			210		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-30V, R_L=3.8\Omega$ $I_D \equiv -15.0A, V_{GEN}=-10V$ $R_G=1.0\Omega$		45	80	ns
	t_r			220	380	
Turn-Off Time	$t_{d(off)}$			95	185	
	t_f			110	200	

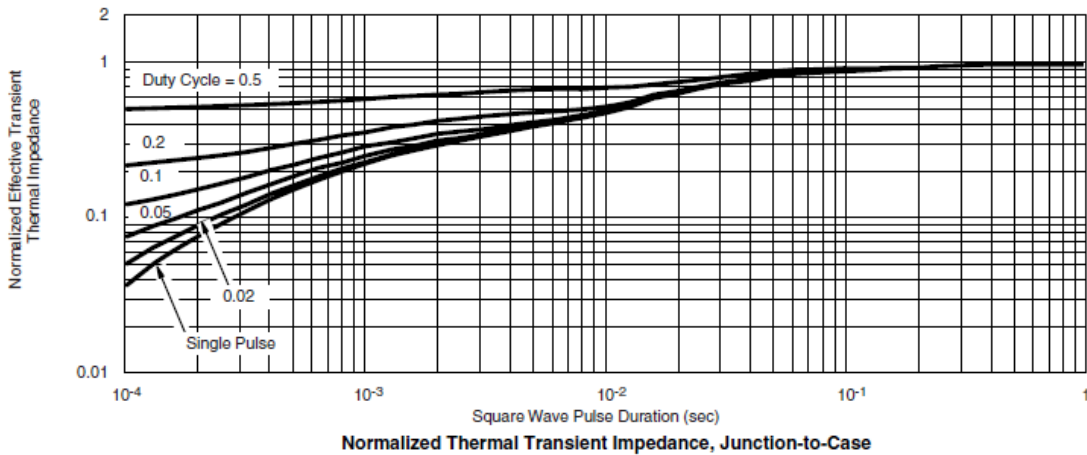
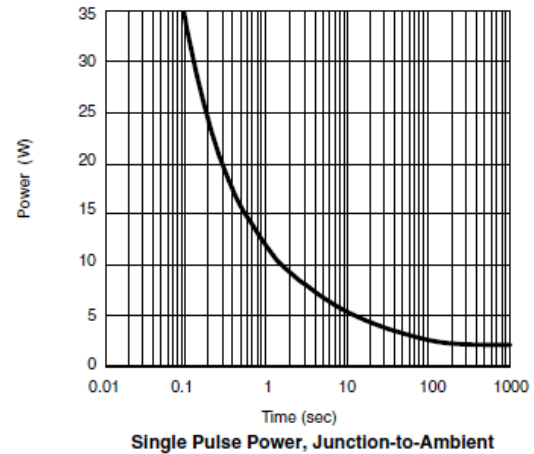
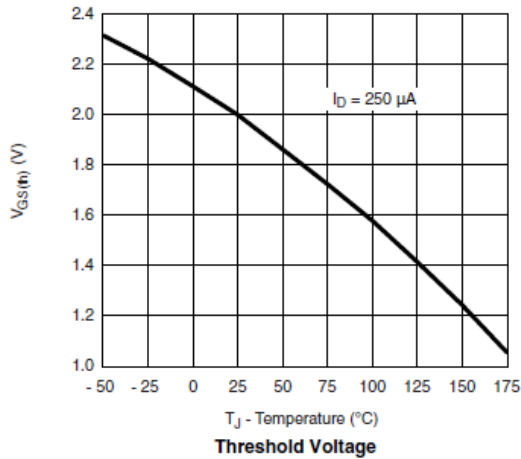
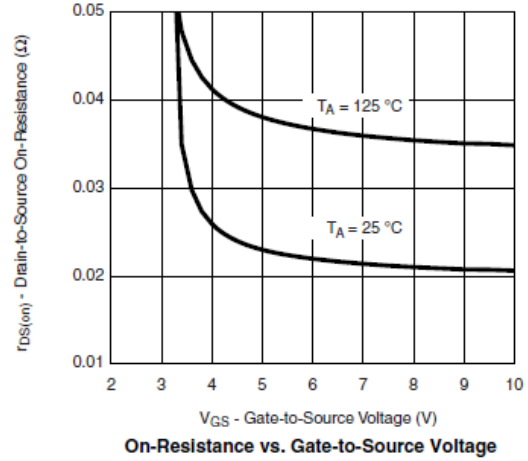
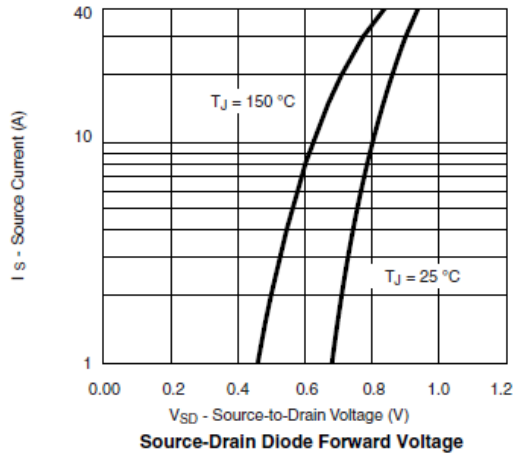


Typical Characteristics





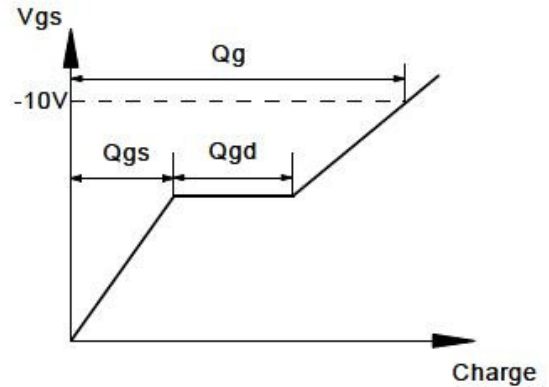
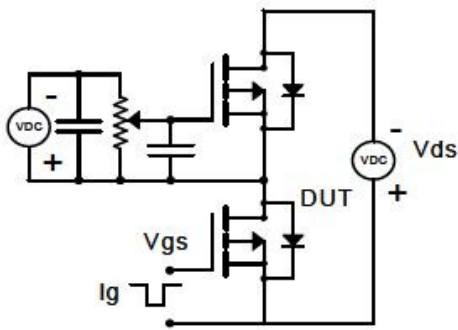
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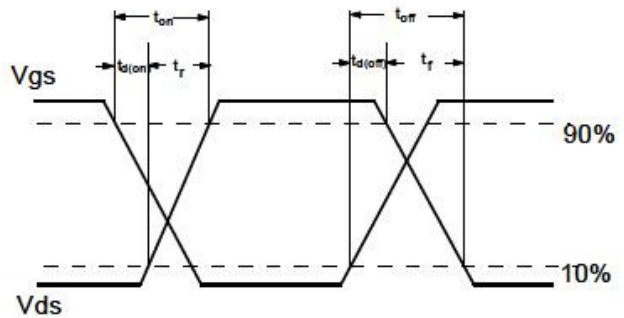
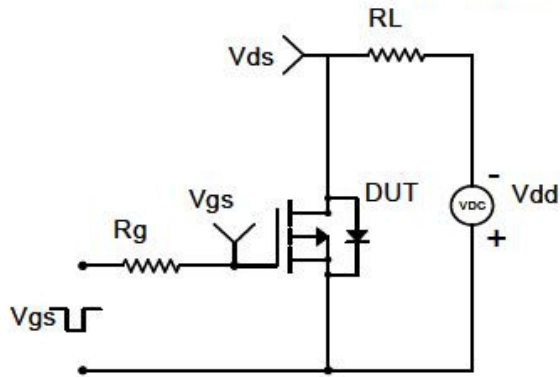


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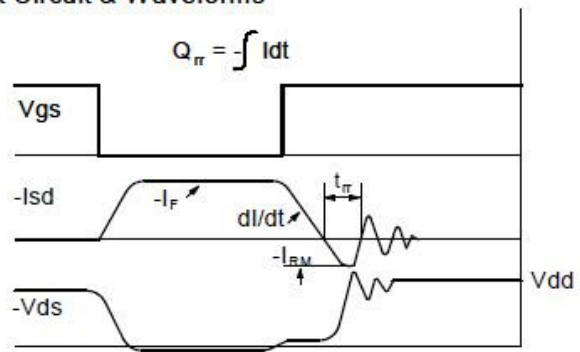
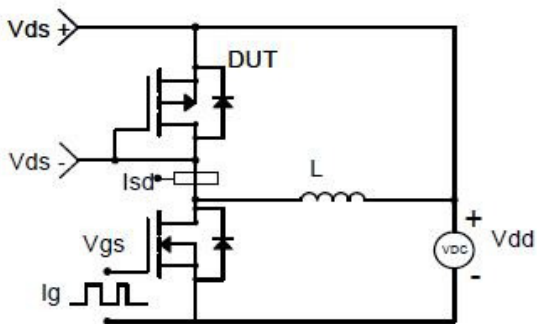
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

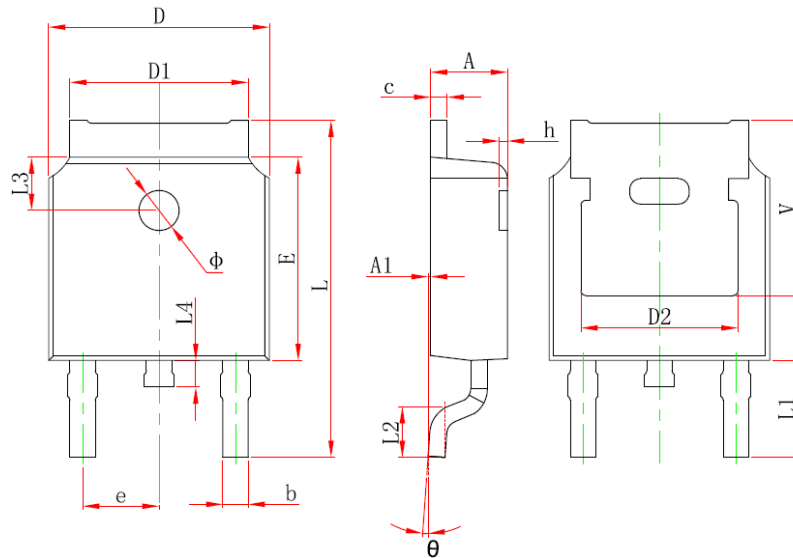


Diode Recovery Test Circuit & Waveforms





Package Information (TO-252-2L)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 REF.		0.211 REF.	

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